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APPEAL BRIEF

Applicants	:	William B. Boyle
App. No	:	09/747,002
Filed	:	December 22, 2000
For	:	METHOD AND APPARATUS FOR STORING A STREAM OF VIDEO DATA ON A STORAGE MEDIUM
Examiner	:	Jamie J. Vent
Art Unit	:	2616

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant (Appellant) is appealing the rejection of Claims 17-29 of the present application as stated in the Final Office Action mailed on October 20, 2006. The rejected claims were also previously rejected in the Final Office Action mailed on September 13, 2005.

This Appeal Brief is being filed within three months from the mailing of the "Notice of Panel Decision from Pre-Appeal Brief Review" on May 10, 2007. Enclosed with the Appeal Brief is the fee set forth in 37 C.F.R. § 41.20(b)(2), along with the fee for a two-month extension. If any fees are due, please charge any additional fees, including any fees for additional extensions of time, or credit overpayment to Deposit Account No. 11-1410.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest of the present application is the Assignee, Keen Personal Media, Inc., a subsidiary of Western Digital Corporation of Lake Forest, California.

II. RELATED APPEALS AND INTERFERENCES

Appellant hereby notify the Board of Patent Appeals that Appellant, the Appellant's Legal Representative, and the Assignee do not know of any other prior or pending appeals, interferences, or judicial proceedings which may be related to, directly affect or be directly affected by or have any bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 17-29 are currently pending in the application, and Claims 1-16 have been previously canceled without prejudice. A copy of the claims is attached hereto as an appendix. All of the pending claims were finally rejected by the Examiner in the Final Office Action mailed October 20, 2006. Rejected Claims 17-29, as they stand rejected in the October 20, 2006 Final Office Action, are the subject of this appeal.

IV. STATUS OF AMENDMENTS

Appellant has not proposed any amendments to the claims subsequent to the October 20, 2006 Final Office Action. Therefore, Claims 17-29 are currently pending.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to systems and methods for storing an video data stream on a storage medium.

Claim 17 recites a method of storing a video data stream on a hard disk drive (HDD) for efficient, non-sequential access to the stored stream of video data. The HDD has a plurality of sectors, with each sector having a first integer of user data bytes. The HDD is addressable on sector boundaries for non-sequential access. The video data stream includes a sequence of original transport packets, with each original transport packet having a second integer of bytes, the second integer of bytes different from the first integer of user data bytes. A third integer of

original transport packets are storable in a fourth integer of sectors, with the fourth integer being a minimum number of sectors with the same number of user data bytes as the number of bytes in the third integer of original transport packets.

An example embodiment of the method is shown in the flowchart of Figure 2 of the application. For the example embodiment shown in Figure 2, in a step 30, the method receives the sequence of original transport packets. (*See, e.g.*, page 5, lines 15-18.) For the example embodiment shown in Figure 2, in a step 32, the method adds a fifth integer of bytes to each original transport packet to create a sequence of modified transport packets, with each modified transport packet having a sixth integer of bytes. (*See, e.g.*, page 5, lines 19-23.) For the example embodiment shown in Figure 2, in a step 34, the method stores the sequence of modified transport packets on the HDD. (*See, e.g.*, page 5, lines 24-27.) A seventh integer of modified transport packets are stored in an eighth integer of sectors, with the eighth integer being a minimum number of sectors with the same number of user data bytes as the number of bytes in the seventh integer of modified transport packets, with the eighth integer of sectors smaller than the fourth integer of sectors. (*See, e.g.*, page 5, line 24 – page 6, line 6.)

Claim 26 recites a system for storing video data for efficient, non-sequential access to the stored video data. An example embodiment of the system is schematically illustrated by Figure 1 of the application. For the example embodiment schematically illustrated by Figure 1, the system 1 comprises a receiver (*e.g.*, data line 14) configured to receive a stream of video data (*e.g.*, from set-top box 6). (*See, e.g.*, page 4, line 29 – page 5, line 7). The stream of video data includes a sequence of original transport packets, wherein each original transport packet has a first predetermined number of bytes. (*See, e.g.*, page 5, lines 15-18.) For the example embodiment schematically illustrated by Figure 1, the system 1 further comprises a first circuit (*e.g.*, control circuit 10) configured to add a second predetermined number of bytes to each original transport packet to create a modified transport packet having a third predetermined number of bytes. (*See, e.g.*, page 5, lines 19-23.) For the example embodiment schematically illustrated by Figure 1, the system 1 further comprises a hard disk drive (HDD) 8 configured to receive and store each modified transport packet. The HDD is addressable on sector boundaries, with each sector having a predetermined number of user data bytes different from the first

predetermined number of bytes. (*See, e.g.*, page 5, lines 24-27.) For the example embodiment schematically illustrated by Figure 1, the first byte in an original transport packet aligns with a first user data byte in a sector after a first predetermined number of sectors following a previous alignment. (*See, e.g.*, page 5, lines 28-29.) The first byte in a modified transport packet aligns with a first user data byte in a sector after a second predetermined number of sectors following a previous alignment, wherein the second predetermined number of sectors is less than the first predetermined number of sectors. (*See, e.g.*, page 5, line 30 – page 6, line 6.)

Reference numbers are to the present application unless indicated otherwise. The present application at page 2, line 28 – page 9, line 2 and Figures 1-5 illustrate various examples of the claimed invention.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether Claims 17-29 are unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 6,134,384 issued to Okamoto *et al.* ("Okamoto") in view of U.S. Patent No. 6,792,000 issued to Morinaga *et al.* ("Morinaga").

VII. ARGUMENT

Pursuant to M.P.E.P. § 2141 (Eighth Edition, Rev. 5, August 2006), patent examiners carry the responsibility of making sure that "the standard of patentability enunciated by the Supreme Court and Congress is applied in each and every case" (emphasis in original). This duty includes the requirement that the Examiner apply the test for patentability under 35 U.S.C. § 103 as set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 U.S.P.Q. 459 (S.Ct. 1966). This test for patentability includes the following four factual inquiries for determining obviousness:

(A) Determining the scope and contents of the prior art;
(B) Ascertaining the differences between the prior art and the claims in issue;
(C) Resolving the level of ordinary skill in the pertinent art; and
(D) Evaluating evidence of secondary considerations.

Appellant submits that the *Graham* test for patentability under 35 U.S.C. § 103 to the question of obviousness has not been fully applied to Claims 17-29. In particular, Appellant submits that the differences between the prior art and the claims in issue have not been correctly ascertained and that the submitted evidence of secondary considerations for patentability leads to a conclusion of

non-obviousness. In addition, Appellant submits that persons skilled in the art would not be motivated to combine the teachings of Okamoto and Morinaga as suggested by the Examiner. Thus, Appellant further submits that the pending claims are patentable over the cited prior art.

1. Differences between the prior art and the claims in issue

Appellant submits that the differences between the prior art and the claims in issue have not been properly ascertained. "In determining the differences between the prior art and the claims, the question under 35 U.S.C. § 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious." (M.P.E.P. § 2141.02(I), emphasis in original, citing *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 U.S.P.Q. 871 (Fed. Cir. 1983); *Schenck v. Nortron Corp.*, 713 F.2d 782, 218 U.S.P.Q. 698 (Fed. Cir. 1983).) Part of this "subject matter as a whole" analysis is the discovery of the source of a problem, which should always be considered in determining obviousness. (M.P.E.P. § 2141.02(III)).

Claims 17-25

With regard to Claim 17, in the October 20, 2006 Final Office Action, the Examiner asserts that Okamoto discloses all the limitations of Claim 17, except for "storing [the] video data stream on a hard disk drive." (October 20, 2006 Final Office Action at page 5, lines 7-11.) The Examiner further asserts that Morinaga discloses "a data processing apparatus wherein transport streams are recorded onto various recording mediums ... by storing the packets on a non-sequential access storage medium, hard disk." (October 20, 2006 Final Office Action at page 5, lines 12-16.) The Examiner concludes that it would have been obvious to one of ordinary skill in the art at the time of the invention to use the recording/reproducing apparatus, as disclosed by Okamoto, and to incorporate a system that stores the transport packets onto a hard disk drive, as disclosed by Morinaga. (October 20, 2006 Final Office Action at page 5, lines 16-20.) In the November 17, 2006 Advisory Action, the Examiner reaffirms this analysis, stating that "it is an obvious design choice of using a hard disk drive, as taught by Morinaga et al, ... for accomplishing storing of data such as transport streams, as disclosed by Okamoto et al." (November 17, 2006 Advisory Action at page 2, lines 9-12.)

Appellant submits that by characterizing the difference between the claimed invention of Claim 17 and the prior art as merely "an obvious design choice," this analysis improperly limits the focus to a structural difference and fails to consider Claim 17 as a whole as required under the *Graham* test for patentability.

Prior systems for storing and accessing video data from hard disk drives suffer from periods of stream discontinuity and loss of synchronization during trick play functions. (*See, e.g.*, present application at page 2, lines 22-25.) As described in the "Declaration of William B. Boyle Pursuant to 37 C.F.R. § 1.132" submitted with the "Response to November 17, 2005 Advisory Action," the claimed invention recited by Claim 17 is a method of storing a video data stream on a hard disk drive with more frequent alignment of the stored modified transport packets with the first bytes of the sectors. Since the hard disk drive is non-sequentially addressable on boundaries between the sectors, this more frequent alignment advantageously allows the system to more efficiently access the stored video data and to enable "trick play" functions without loss of synchronization. (*See, e.g.*, present application at page 6, lines 7-11 and page 7, lines 20-25.) This insight regarding the source of the problem and its solution is not provided by the prior art. In addition, this solution of adding non-video bytes of data (in some cases, adding merely null data bytes) to the transport packets results in more storage space being used to store the video program than would otherwise be needed, which is contrary to the conventional desire to maximize the amount of video data stored on a given storage capacity. Therefore, the claimed invention of Claim 17, when properly considered as a whole, would not have been obvious to those skilled in the art, and so is patentably distinguished over the prior art.

Each of Claims 18-25 depends either directly or indirectly from Claim 17, so for at least the reasons stated with regard to Claim 17, Appellant submits that Claims 18-25 are each patentably distinguished over the prior art.

Claims 26-29

With regard to Claim 26, in the October 20, 2006 Final Office Action, the Examiner asserts that Okamoto discloses "a system for storing video data for efficient non-sequential access to stored video data as previously disclosed in Claim 17," but that Okamoto fails to disclose "[a] receiver configured to receive a stream of video data that includes a sequence of

original transport packets." (October 20, 2006 Final Office Action at page 7, lines 11-16.) The Examiner further asserts that Morinaga discloses "a receiver ... wherein the transport packets are descrambled and identified." (October 20, 2006 Final Office Action at page 7, lines 18-20.) The Examiner concludes that it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate a receiver as disclosed by Morinaga in the system disclosed by Okamoto. (October 20, 2006 Final Office Action at page 7, line 22 – page 8, line 3.)

Appellant submits that this analysis fails to consider Claim 26 as a whole as required by the *Graham* test of patentability. Appellant submits that this analysis completely ignores features recited by Claim 26, namely:

> a hard disk drive (HDD) configured to receive and store each modified transport packet, wherein the HDD is addressable on sector boundaries, each sector having a predetermined number of user data bytes different from the first predetermined number of bytes, wherein:
>
> the first byte in an original transport packet aligns with a first user data byte in a sector after a first predetermined number of sectors following a previous alignment; and
>
> the first byte in a modified transport packet aligns with a first user data byte in a sector after a second predetermined number of sectors following a previous alignment, wherein the second predetermined number of sectors is less than the first predetermined number of sectors.

Appellant submits that by omitting consideration of all the features recited by Claim 26, this analysis fails to consider the claimed invention as a whole. (*See*, M.P.E.P. § 2143.03; *In re Wilson*, 424 F.2d 1382, 1385, 165 U.S.P.Q. 494, 496 (CCPA 1970)("All words in a claim must be considered in judging the patentability of that claim against the prior art.")).

While the Examiner may have been relying on the previously-described analysis regarding Claim 17 for the proposition that the hard disk drive is "an obvious design choice," Appellant submits that this analysis still ignores the features recited by Claim 26 regarding the alignment of the first byte in the original transport packet and the modified transport packet. Furthermore, as discussed above with regard to Claim 17, Appellant submits that by characterizing the difference between the claimed invention of Claim 26 and the prior art as merely "an obvious design choice" in the November 17, 2005 Advisory Action, this analysis fails to consider Claim 26 as a whole as required under the *Graham* test for patentability.

Appellant further submits that the claimed invention of Claim 26, when properly considered as a whole, would not have been obvious to those skilled in the art, and so is patentably distinguished over the prior art.

Each of Claims 27-29 depends either directly or indirectly from Claim 26, so for at least the reasons stated with regard to Claim 26, Appellant submits that Claims 27-29 are each patentably distinguished over the prior art.

2. Submitted evidence of non-obviousness

Appellant has previously timely submitted a "Declaration of William B. Boyle Pursuant to 37 C.F.R. § 1.132" ("the Declaration") in which evidence of non-obviousness was provided. Pursuant to M.P.E.P. § 716.01(a), such timely presented objective evidence of non-obviousness must be considered by the Examiner. Merely providing a statement that the evidence has been considered and has been found unconvincing is insufficient; the Examiner should identify the reasons for such a conclusion. M.P.E.P. § 716.01(d). If the evidence is insufficient to overcome the rejection, "the examiner must specifically explain why the evidence is insufficient" (emphasis added), and "[g]eneral statements ... without an explanation supporting such findings are insufficient." M.P.E.P. § 716.01(d). Appellant submits that this submitted evidence has not been fully considered by the Examiner, and that proper consideration of this evidence leads to a conclusion of non-obviousness of the claimed invention.

Unexpected results

A claim is non-obvious over the prior art where it does "more than yield a predictable result." (*KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. ___, 12 (2007), citing *U.S. v. Adams*, 383 U.S. 39 (1966)). As described in paragraph 8 of the Declaration, the method and system of Claims 17 and 26 provide results which are unexpected from the combination of Okamoto and Morinaga. As disclosed by the present application at page 6, lines 7-11, the claimed method recited by Claim 17 and claimed system of Claim 26 provide modified transport packets which "align[] more often with the first byte of a sector so that the system 1 can more efficiently access the video data" stored on the hard disk drive and to enable "trick play" functions without loss of synchronization. This more frequent alignment and smaller cluster size "provides for more efficient access to the stored video data because the synchronization performance is improved

and repeated re-locking of a decoder ... is avoided." (*See*, present application at page 7, lines 20-25). The Declaration explains that "neither Okamoto nor Morinaga discloses or suggests such an advantage, and persons skilled in the art would not expect such an advantage from the combination of Okamoto in view of Morinaga." Thus, the method and system recited by Claims 17 and 26 provide benefits which are unexpected in view of the prior art. Therefore, proper consideration of this evidence of non-obviousness leads to the conclusion that Claims 17-29 are patentably distinguished over the cited prior art.

Appellant notes that the Examiner has not provided any comments on the sufficiency of the evidence of unexpected results, despite the requirement to weigh such evidence against evidence supporting *prima facie* obviousness in making a final determination of the obviousness of the claimed invention. M.P.E.P. § 716.02(c). However, accompanying the "Notice of Panel Decision from Pre-Appeal Brief Review" on May 10, 2007 was an Office communication from the Examiner which reads in its entirety: "The Declaration filed 12/20/05 has been considered in the last Office Action." Appellant submits that this minimal statement does not provide any reasons for deviating from the conclusion of non-obviousness reached above.

Change of the principles of operation of the prior art

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." M.P.E.P. § 716.02(c), citing *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (CCPA 1959). As described in paragraph 7 of the Declaration, due to the differences between the sequentially-accessed magnetic tape of Okamoto and the non-sequentially accessed hard disk drive of Morinaga, including differences in the data formats of these two types of media, the substitution of the hard disk drive disclosed by Morinaga for the magnetic tape disclosed by Okamoto would require changes of the data formats, the mechanisms for recording and reproducing signals, and the error correction codes disclosed by Okamoto. Thus, modifying the teaching of Okamoto with the teaching of Morinaga would require a substantial reconstruction and redesign of the elements disclosed by Okamoto as well as a change in the basic principle under which the system and method of Okamoto was designed to operate.

Therefore, the combination of Okamoto in view of Morinaga is not sufficient to render the claimed invention obvious.

3. No motivation to combine the cited references

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention when there is an apparent reason at the time of the invention for persons skilled in the art to combine the prior art elements in the fashion claimed by the patent application at issue. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. ___, 14-15 (2007). Appellant submits that at the time of the invention, there was no reason for persons skilled in the art to combine the teachings of Okamoto and Morinaga to produce the method and system recited by Claims 17 and 26.

Okamoto discloses a particular error correction code system and method designed to deal with the particular problems associated with digital signal recording onto magnetic tape. Morinaga discloses a data processing apparatus and method utilizing a hard disk drive. Appellant submits that neither Okamoto nor Morinaga discloses any motivation to combine the hard disk drive of Morinaga with the method and apparatus taught by Okamoto. Furthermore, the Examiner has not identified any reason at the time of the invention for persons skilled in the art to produce such a combination. Therefore, persons skilled in the art would not have had a reason to modify the method of Okamoto with the teachings of Morinaga.

In the October 20, 2006 Final Office Action, the Examiner asserts that it is well known that many storage medium "are available for" storing data. The Examiner further asserts that various prior art references show that "a system can have various mediums for storing data" (emphasis added). However, Appellant submits that the mere fact that references can be combined does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *See In re Mills*, 916 F.2d 680 (Fed. Cir. 1990). To support the Examiner's assertion of obviousness, the Examiner must provide clear and particular findings as to the reason one skilled in the art, with no knowledge of the claimed invention, would have selected these components and combined them in the manner claimed. *See, e.g., In re Kotzab*, 217 F.3d 1365, 1371 (Fed. Cir. 2000). The assertion by the Examiner of obviousness without identifying such a teaching or suggestion in the prior art of the desirability of the combination is

an impermissible use of hindsight derived from the teachings of the present application. *See, e.g., In re Dembiczak*, 175 F.3d 994, 999 (Fed. Cir. 1999).

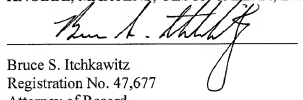
Appellant therefore submits that Claims 17-29 are patentably distinguished over the combination of Okamoto in view of Morinaga.

Conclusion

In view of the foregoing, Appellant respectfully submits that the rejections of Claims 17-29 are not well founded. Appellant therefore respectfully requests that the Board reverse the rejection of Claims 17-29.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP



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VIII. CLAIMS APPENDIX

1.-16. (Canceled)

17. A method of storing a video data stream on a hard disk drive (HDD) for efficient, non-sequential access to the stored stream of video data, the HDD having a plurality of sectors, each sector having a first integer of user data bytes, the HDD addressable on sector boundaries for non-sequential access, the video data stream including a sequence of original transport packets, each original transport packet having a second integer of bytes, the second integer of bytes different from the first integer of user data bytes, wherein a third integer of original transport packets are storable in a fourth integer of sectors, the fourth integer being a minimum number of sectors with the same number of user data bytes as the number of bytes in the third integer of original transport packets, the method comprising:

receiving the sequence of original transport packets;

adding a fifth integer of bytes to each original transport packet to create a sequence of modified transport packets, each modified transport packet having a sixth integer of bytes; and

storing the sequence of modified transport packets on the HDD, wherein a seventh integer of modified transport packets are stored in an eighth integer of sectors, the eighth integer being a minimum number of sectors with the same number of user data bytes as the number of bytes in the seventh integer of modified transport packets, the eighth integer of sectors smaller than the fourth integer of sectors.

18. The method of Claim 17, wherein the second integer of bytes is 188.

19. The method of Claim 18, wherein the fifth integer of bytes is four so that the sixth integer of bytes is 192.

20. The method of Claim 17, wherein the second integer of bytes is 188 and wherein the fifth integer of bytes is four so that each modified transport packet has a length of 192 bytes.

21. The method of Claim 20, wherein the first integer of user data bytes is 512, and wherein the eighth integer of sectors is three.

22. The method of Claim 17, wherein the first integer of user data bytes is 512.

23. The method of Claim 17, wherein each original transport packet includes synchronization bytes located at a beginning of each original transport packet, and wherein the fifth integer of bytes is added in front of the synchronization bytes.

24. The method of Claim 17, wherein each original transport packet includes synchronization bytes located at a beginning of each original transport packet, and wherein the fifth integer of bytes is inserted behind the synchronization bytes.

25. The method of Claim 17, further comprising passing each modified transport packet through a first buffer prior to storing on the HDD.

26. A system for storing video data for efficient, non-sequential access to the stored video data, the system comprising:

a receiver configured to receive a stream of video data that includes a sequence of original transport packets, wherein each original transport packet has a first predetermined number of bytes;

a first circuit configured to add a second predetermined number of bytes to each original transport packet to create a modified transport packet having a third predetermined number of bytes; and

a hard disk drive (HDD) configured to receive and store each modified transport packet, wherein the HDD is addressable on sector boundaries, each sector having a predetermined number of user data bytes different from the first predetermined number of bytes, wherein:

the first byte in an original transport packet aligns with a first user data byte in a sector after a first predetermined number of sectors following a previous alignment; and

the first byte in a modified transport packet aligns with a first user data byte in a sector after a second predetermined number of sectors following a previous alignment, wherein the second predetermined number of sectors is less than the first predetermined number of sectors.

27. The system of Claim 26, further comprising a second circuit configured to remove the second predetermined number of bytes from each modified transport packet retrieved from the HDD.

28. The system of Claim 26, wherein the first predetermined number of bytes is 188 and wherein the second predetermined number of bytes is four so that the third number of bytes is 192 bytes.

29. The system of Claim 28, wherein the predetermined number of user data bytes is 512, and wherein the second predetermined number of sectors is three.

IX. EVIDENCE APPENDIX

1. U.S. Patent No. 6,134,384 issued to Okamoto *et al.* ("Okamoto"); cited by the Examiner in the October 20, 2006 Final Office Action and the November 17, 2006 Advisory Action.
2. U.S. Patent No. 6,792,000 issued to Morinaga *et al.* ("Morinaga"); cited by the Examiner in the October 20, 2006 Final Office Action and the November 17, 2006 Advisory Action.
3. "Declaration of William B. Boyle Pursuant to 37 C.F.R. § 1.132;" submitted with the "Response to November 17, 2005 Advisory Action" and acknowledged as being entered in the record by the Examiner in the Office Communication accompanying the "Notice of Panel Decision from Pre-Appeal Brief Review" on May 10, 2007.

X. RELATED PROCEEDINGS APPENDIX

None.

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061007

US006134384A

United States Patent [19]

Okamoto et al.

[11] Patent Number: 6,134,384

[45] Date of Patent: Oct. 17, 2000

[54] **DIGITAL SIGNAL RECORDING/ REPRODUCING APPARATUS AND RECORDING METHOD**

[75] Inventors: **Hiroo Okamoto; Takaharu Noguchi; Hitoaki Owashi,** all of Yokohama, Japan

[73] Assignee: **Hitachi, Ltd.,** Tokyo, Japan

[21] Appl. No.: **08/810,070**

[22] Filed: **Mar. 4, 1997**

[30] **Foreign Application Priority Data**

Mar. 4, 1996 [JP] Japan 8-045804
Mar. 5, 1996 [JP] Japan 8-047078

[51] **Int. Cl.**[7] **H04N 5/911**

[52] **U.S. Cl.** **386/116**; 360/124; 360/32

[58] **Field of Search** 386/109, 112, 386/113, 114, 116, 83, 124; 360/32, 99

[56] **References Cited**

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Primary Examiner—Wendy Garber
Assistant Examiner—Christopher Onuaku
Attorney, Agent, or Firm—Antonelli, Terry, Stout & Kraus, LLP

[57] **ABSTRACT**

An apparatus and method for recording on and reproducing from a magnetic tape a digital signal by rotating heads. A synchronizing signal, a control signal, and an error correction code are added to the digital signal, and the digital signal with those signals added is converted into a block form. At the recording time, a recording signal produced from a recording circuit is recorded on the recording medium by a first head of the rotating heads, and at the same time the recorded signal is reproduced by a second head of the rotating heads. In addition, there are provided a first recording mode in which two error correction codes are added, and a second recording mode in which three error correction codes are added. Thus, the recorded signal can be confirmed by the simultaneous playback made at the recording time so that the reliability in data can be assured.

16 Claims, 12 Drawing Sheets

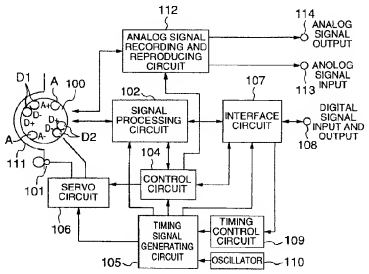
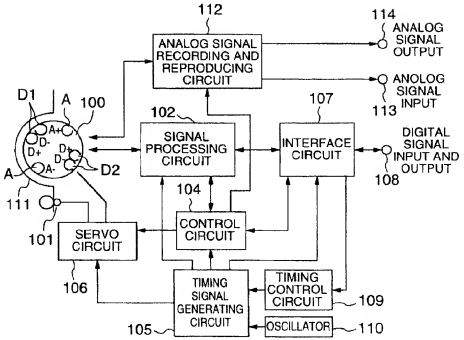


FIG.1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114
ANALOG SIGNAL RECORDING AND REPRODUCING CIRCUIT
ANALOG SIGNAL OUTPUT
ANOLOG SIGNAL INPUT
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A+
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D+
D1
D2
A-
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SIGNAL PROCESSING CIRCUIT
INTERFACE CIRCUIT
DIGITAL SIGNAL INPUT AND OUTPUT
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TIMING SIGNAL GENERATING CIRCUIT
TIMING CONTROL CIRCUIT
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OSCILLATOR
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FIG.2

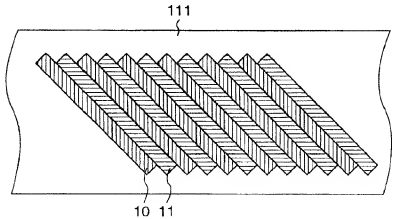
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FIG.3

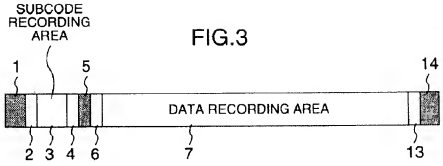


FIG.4A

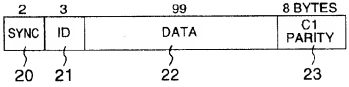


FIG.4B

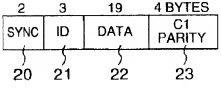


FIG.5

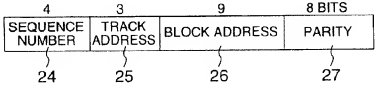


FIG.6

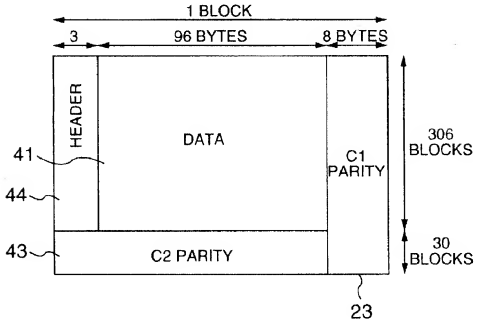

1 BLOCK
3
96 BYTES
8 BYTES
HEADER
DATA
C1 PARITY
306 BLOCKS
41
44
43
C2 PARITY
30 BLOCKS
23

FIG.7

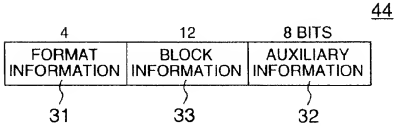

44
4
12
8 BITS
FORMAT INFORMATION
BLOCK INFORMATION
AUXILIARY INFORMATION
31
33
32

FIG.8

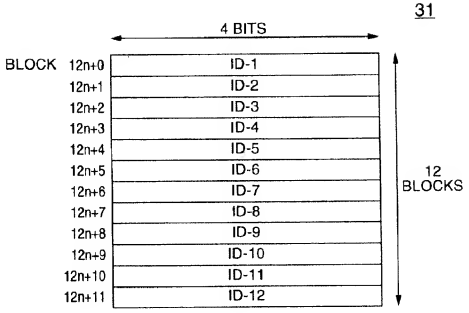

31
4 BITS
BLOCK
12n+0
12n+1
12n+2
12n+3
12n+4
12n+5
12n+6
12n+7
12n+8
12n+9
12n+10
12n+11
ID-1
ID-2
ID-3
ID-4
ID-5
ID-6
ID-7
ID-8
ID-9
ID-10
ID-11
ID-12
12
BLOCKS

FIG.9

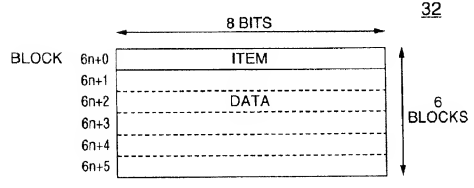

32
8 BITS
BLOCK
6n+0
6n+1
6n+2
6n+3
6n+4
6n+5
ITEM
DATA
6
BLOCKS

FIG.10

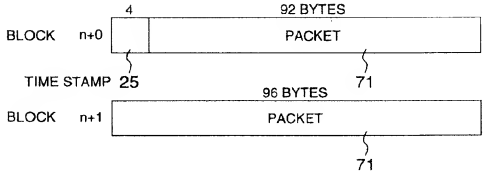

4
92 BYTES
BLOCK n+0
PACKET
TIME STAMP 25
71
96 BYTES
BLOCK n+1
PACKET
71

FIG.11

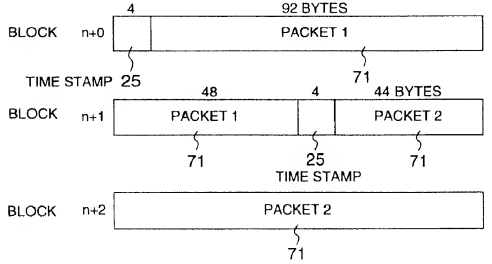

4
92 BYTES
BLOCK n+0
PACKET 1
TIME STAMP 25
71
48
4
44 BYTES
BLOCK n+1
PACKET 1
PACKET 2
71
25
71
TIME STAMP
BLOCK n+2
PACKET 2
71

FIG.12

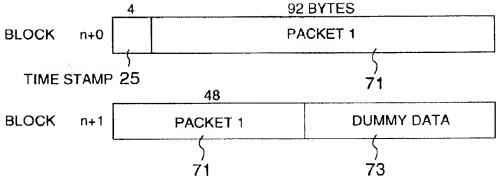


FIG.13

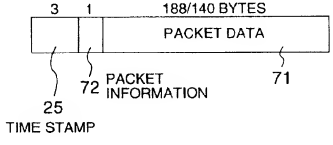


FIG.14

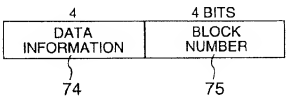


FIG.15

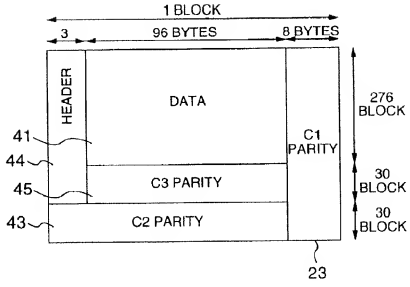

1 BLOCK
3
96 BYTES
8 BYTES
HEADER
DATA
C1 PARITY
C3 PARITY
C2 PARITY
276 BLOCK
30 BLOCK
30 BLOCK
41
44
45
43
23

FIG.16

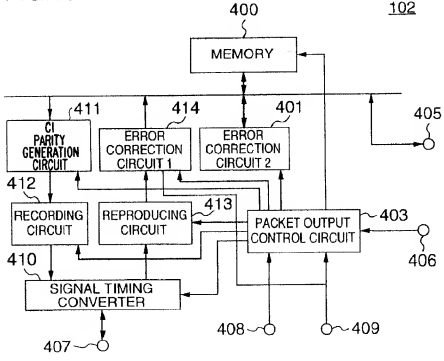

400
102
MEMORY
411
414
401
405
CI PARITY GENERATION CIRCUIT
ERROR CORRECTION CIRCUIT 1
ERROR CORRECTION CIRCUIT 2
412
413
RECORDING CIRCUIT
REPRODUCING CIRCUIT
PACKET OUTPUT CONTROL CIRCUIT
403
406
410
SIGNAL TIMING CONVERTER
408
409
407

FIG.17

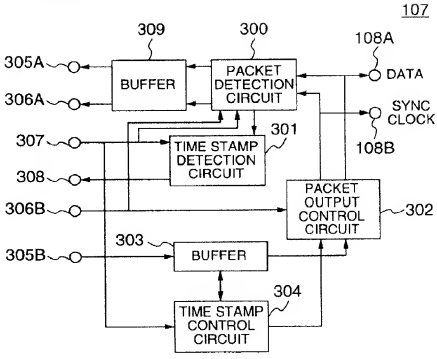


FIG.18

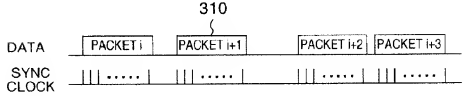


FIG.19

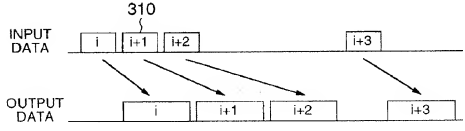


FIG.20

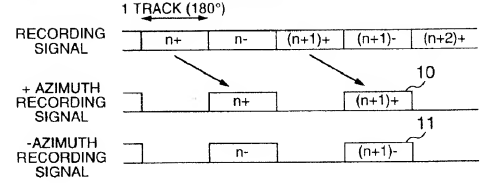


FIG.21

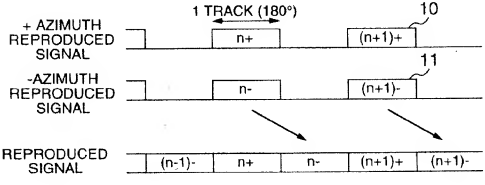


FIG.22

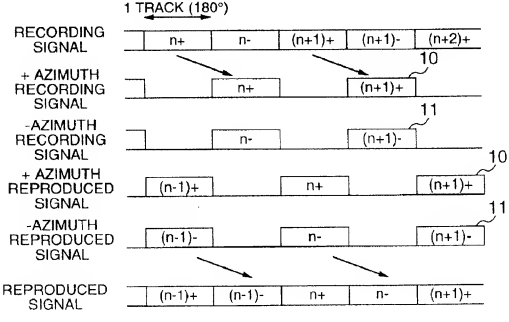


FIG.23

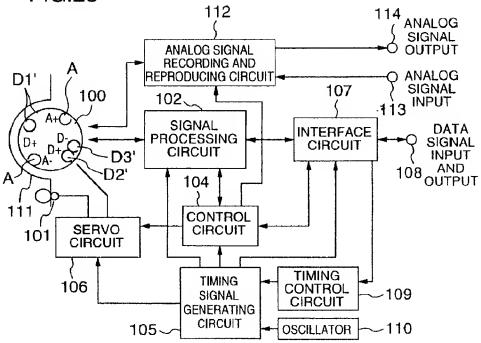

112
114
ANALOG SIGNAL OUTPUT
ANALOG SIGNAL RECORDING AND REPRODUCING CIRCUIT
ANALOG SIGNAL INPUT
113
D1'
A
100
102
107
A+
D-
D+
D+
A-
SIGNAL PROCESSING CIRCUIT
INTERFACE CIRCUIT
DATA SIGNAL INPUT AND OUTPUT
108
D3'
D2'
A
104
111
CONTROL CIRCUIT
101
SERVO CIRCUIT
106
TIMING SIGNAL GENERATING CIRCUIT
TIMING CONTROL CIRCUIT
109
105
OSCILLATOR
110

FIG.24

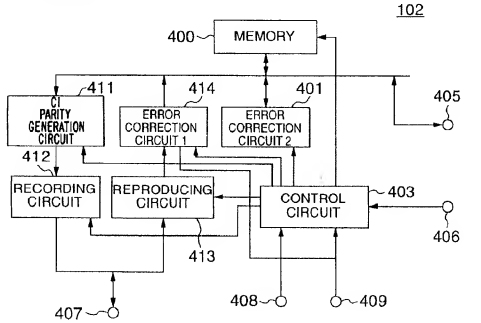

102
400
MEMORY
411
414
401
405
CI PARITY GENERATION CIRCUIT
ERROR CORRECTION CIRCUIT 1
ERROR CORRECTION CIRCUIT 2
412
RECORDING CIRCUIT
REPRODUCING CIRCUIT
CONTROL CIRCUIT
403
406
413
407
408
409

FIG.25

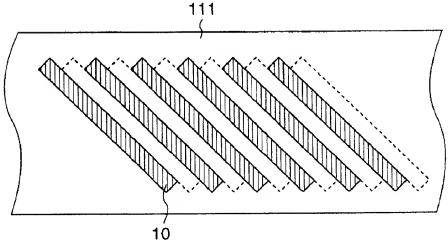

111
10

FIG.26

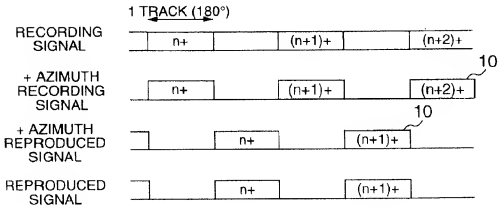

1 TRACK (180°)
RECORDING SIGNAL
+ AZIMUTH RECORDING SIGNAL
+ AZIMUTH REPRODUCED SIGNAL
REPRODUCED SIGNAL
n+
(n+1)+
(n+2)+
10
10

FIG.27

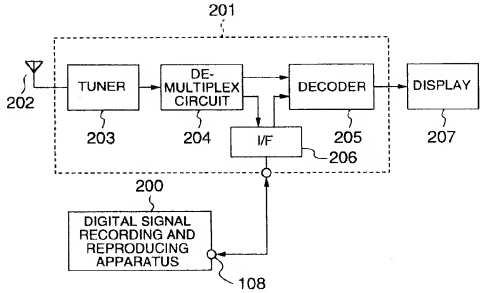
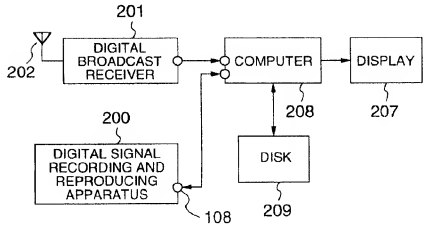

201
202
TUNER
DE-MULTIPLEX CIRCUIT
DECODER
DISPLAY
203
204
I/F
205
206
207
200
DIGITAL SIGNAL RECORDING AND REPRODUCING APPARATUS
108

FIG.28


201
202
DIGITAL BROADCAST RECEIVER
COMPUTER
DISPLAY
208
207
200
DISK
DIGITAL SIGNAL RECORDING AND REPRODUCING APPARATUS
108
209

DIGITAL SIGNAL RECORDING/ REPRODUCING APPARATUS AND RECORDING METHOD

BACKGROUND OF THE INVENTION

The present invention relates to a digital signal recording/reproducing apparatus and recording method for recording and/or reproducing a digital signal, and particularly to a digital signal recording/reproducing apparatus and recording method for recording and/or reproducing a digital signal on a magnetic tape by use of rotating heads.

A digital signal recording apparatus is disclosed in JP-A-5-174496. This apparatus records a digital compressed video signal on a magnetic tape by use of rotating heads. However, there is no consideration about the improvement in the reliability at the time of recording.

SUMMARY OF THE INVENTION

It is an object of the invention to provide a digital signal recording and reproducing apparatus capable of recording and reproducing even digital data that needs high reliability, without increasing the circuit scale

It is another object of the invention to reduce the number of heads and make it unnecessary to use a signal timing converter by use of only one azimuth head when digital data that needs high reliability is recorded and reproduced.

It is still another object of the invention to increase the storage capacity and raise the reliability by use of two or three error correction codes according to the intention.

According to the present invention, there is provided a digital signal recording and reproducing apparatus for recording on and reproducing from each of tracks, or digital signal recording areas of a magnetic recording medium a plurality of blocks each consisting of a digital signal, and added signals of a synchronizing signal, a control signal and an error correction code, this apparatus including a memory for storing the digital signal fed at the time of recording or produced at the time of reproduction, error correction code adding circuits for adding error correction codes to the digital signal stored in the memory, a recording circuit for making a block-type signal of the blocks from the digital signal with the error correction codes added by the error correction code adding circuit, a reproducing circuit for detecting the digital signal and the error correction codes from a reproduced signal, error correction circuits for detecting and correcting error of the digital signal on the basis of the error correction codes detected by the reproducing circuit, and a plurality of rotating heads for recording and reproduction, whereby at the recording time a recording signal produced from the recording circuit is recorded on the recording medium by a first head of the rotating heads, the recorded signal is reproduced by a second head of the rotating heads at the same time as the recording time so that the reproducing circuit and the error correction circuits can detect error from the reproduced signal, and at the playback time the recorded signal is reproduced by the first head, the resulting reproduced signal being fed to the memory after error detection by the reproducing circuit and the error correction circuits.

In addition, according to the present invention, there is provided a digital signal recording method and apparatus for recording on each of tracks, or digital signal recording areas of a magnetic recording medium a plurality of blocks each consisting of a digital signal, and added signals of a synchronizing signal, a control signal and an error correction code, this method and apparatus having a first recording mode for adding a first error correction code to each n tracks (n is an integer larger than 1) of the digital signal, adding a second error correction code to each block of the digital signal and the first error correction code, and recording the digital signal with the first and second error correction codes added, and a second recording mode for adding a third error correction code to each n tracks of the digital signal, adding a fourth error correction code to each track of the digital signal and the third error correction code, adding a second error correction code to each block of the digital signal, the third error correction code and the fourth error correction code, and recording the digital signal with the second, third and fourth error correction codes added.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the present invention will now be described in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram of the first embodiment of a digital signal recording and reproducing apparatus according to the invention;

FIG. 2 is a diagram of a pattern recorded on a magnetic tape;

FIG. 3 is a diagram of a recorded pattern of each track;

FIGS. 4A and 4B are diagrams of blocks in respective regions;

FIG. 5 is a diagram of the format of the ID information **21** shown in FIGS. 4A and 4B;

FIG. 6 is a diagram of the structure of one-track data in the data recording area **7** shown in FIG. 3;

FIG. 7 is a diagram of the header **44** of the data recording area **7** shown in FIG. 3;

FIG. 8 is a diagram of the format of the format information **31** shown in FIG. 7;

FIG. 9 is a diagram of the format of the auxiliary information **32** shown in FIG. 7;

FIG. **10** is a diagram of the format of blocks of a digital compressed video signal transmitted in the form of a packet of 188 bytes, these blocks being recorded in the data recording area **41** shown in FIG. 6;

FIG. 11 is a diagram of one format of blocks of which the packet **71** has a length of 140 bytes;

FIG. **12** is a diagram of another format of blocks of which the packet **71** has a length of 140 bytes;

FIG. 13 is a diagram of another format of the packet shown in FIG. **10**, **11** or **12**;

FIG. 14 is a diagram of the format of the block information **33** shown in FIG. **7**;

FIG. 15 is a diagram of the format of one-track data in the data recording area **7** in which digital data is recorded;

FIG. **16** is a block diagram of the signal processing circuit **102** in FIG. 1;

FIG. **17** is a block diagram of the interface circuit **107** in FIG. 1;

FIG. **18** is a timing diagram of an input/output signal,

FIG. **19** is a timing diagram of input to and output from the buffer **309** in FIG. 17;

FIG. **20** is a timing diagram of the operation of the signal timing converter **410** at the time of recording in FIG. 16;

FIG. **21** is a timing diagram of the operation of the signal timing converter **410** at the time of reproduction in FIG. 16;

FIG. **22** is a timing diagram of the operation of the signal timing converter **410** at the time of recording digital data in FIG. 16;

FIG. **23** is a block diagram of the second embodiment of a digital signal recording and reproducing apparatus according to the invention;

FIG. **24** is a block diagram of the signal processing circuit **102** of the digital signal recording and reproducing apparatus in FIG. **23**;

FIG. **25** is a diagram of a pattern recorded on a magnetic tape by the digital signal recording and reproducing apparatus of FIG. **23**;

FIG. **26** is a timing diagram of recording and reproduction in the digital signal recording and reproducing apparatus of FIG. **23**;

FIG. **27** is a block diagram of the digital signal recording and reproducing apparatus and a digital broadcast receiver which are connected to each other; and

FIG. **28** is a block diagram of the digital signal recording and reproducing apparatus and a computer which are connected to each other.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the invention will be described with reference to the accompanying drawings.

FIG. **1** is a block diagram of a digital signal recording and reproducing apparatus according to the invention. The digital signal recording and reproducing apparatus in FIG. **1** is constructed for both recording and reproduction, but may be, of course, arranged for either recording or reproduction. There are shown rotating heads **100**, a capstan **101**, a signal processing circuit **102** for generating a recording signal at the time of recording and demodulating a reproduced signal at the time of reproduction, a control circuit **104**, such as a microprocessor, for controlling the recording and reproduction modes, a timing signal generating circuit **105** for generating timing signals that are used as reference signals for controlling the rotation of heads **100** and for other purposes, and a servo circuit **106** for controlling the rotating heads and the tape transport speed. There are also shown an interface circuit **107** to which a recording signal is fed or from which a reproduced signal is produced, a timing control circuit **109** for controlling the timing at the time of recording, an oscillator **110** for generating a reference clock, a tape **111**, and an analog signal recording and reproducing circuit for an analog video signal. The rotating heads **100** include first and second heads D1, D2 (D+, D−) for recording and reproducing a digital signal, and heads A (A+, A−) for recording and reproducing an analog signal.

At the time of recording, recording data of a packet form are supplied via an input/output terminal **108** at arbitrary intervals of time. A part of the packet data from the input/output terminal **108** is supplied through the interface circuit **107** to the control circuit **104**. The control circuit **104** detects the kind of packet data and the maximum transmission rate on the basis of information added to the packet data or information transmitted independently of the packet data, decides a recording mode according to the detected result, and controls the signal processing circuit **102** and the servo circuit **106** to operate in a certain mode. The interface circuit **107** detects the packet data being recorded, and supplies it to the signal processing circuit **102**. The signal processing circuit **102** is responsive to the recording mode decided at the control circuit **104** to decide the number of packets being recorded on one track, generates error correction codes, ID information and subcodes, and supplies a recording signal to the rotating heads **100** by which the signal is recorded on the magnetic tape **111**.

At the time of reproduction, the recorded signal is reproduced in an arbitrary reproduction mode, and the signal processing circuit **102** detects ID information from the reproduced signal. The control circuit **104** decides which mode the signal was recorded in, and controls the signal processing circuit **102** and servo circuit **106** to be set to a new operation mode, causing the heads to reproduce the recorded signal. The signal processing circuit **102** detects the synchronizing signal, makes error detection and correction, and reproduces data and subcodes on the basis of the reproduced signal from the heads **100**, and it supplies them to the interface circuit **107**. The interface circuit **107** produces the reproduced data at its input/output terminal **108** according to the timing signal generated from the timing signal generating circuit **105**.

When an analog video signal is recorded and reproduced, an analog video signal fed via an input terminal **113** at the time of recording is processed in a certain way by the analog signal recording and reproducing circuit **112** and supplied to the rotating heads **100** by which it is recorded on the tape **111**. The reproduced video signal from the rotating heads **100** at the time of reproduction is processed in a certain way by the analog signal recording and reproducing circuit **112**, and then produced at its output terminal **114**. In this case, the servo circuit **106** is controlled in synchronism with the frame period of the analog video signal, though not shown. Although the heads for analog video signal are provided independently of the digital recording heads as seen from FIG. **1**, the digital recording heads may be used both as the analog recording heads and as themselves instead of the analog recording heads or the analog recording heads may be provided independently of the digital recording heads.

The digital signal recording and reproducing apparatus of this embodiment is able to record and reproduce both a digital compressed video signal, and digital data such as a computer program.

First, the recording and reproduction of a digital compressed video signal will be described below.

FIG. **2** shows a recorded pattern on the tape **111**. There are shown +azimuth tracks **10** and −azimuth tracks **11**, which are recorded and reproduced by +azimuth heads (D+) and −azimuth heads (D−), respectively.

FIG. **3** shows a recorded pattern of one track. There are shown a subcode recording area **3** in which a subcode such as time stamp and program information is recorded, a data recording area **7** in which a digital compressed video signal is recorded, preambles **2**, **6** for those recording areas, postambles **4**, **13** for those recording areas, a gap **5** between those recording areas, and margins **1**, **14** at the ends of the track. Thus, by providing the postambles, preambles and gap to those recording areas, it is possible to perform after-recording for each region. Of course, a digital signal other than the digital compressed video signal and audio signal may be recorded in the data recording area **7**. In addition, a digital compressed audio signal may be recorded in the data recording area **7** together with the digital compressed video signal.

FIGS. **4**A and **4**B show the block formats of those regions. FIG. **4**A illustrates the block format in the data recording area **7**. There are shown a synchronizing signal **20**, ID information **21**, data **22**, and a parity (C1 parity) **23** for first error detection and correction. For example, the synchronizing signal **20** is formed of 2 bytes, the ID information **21** of 3 bytes, the data **22** of 99 bytes and the parity **23** of 8 bytes, one block thus consisting of 112 bytes. FIG. **4**B shows the block format in the subcode recording area **3**. The block

in the subcode recording area has the synchronizing signal **20** and ID information **21** of the same bytes as in FIG. **4A**, the data **22** of 19 bytes and the parity **23** of 4 bytes, one block thus consisting of 28 bytes, or ¼ the total bytes of the block in FIG. **4A**. Since the byte number ratio between those one-block regions is an integer and the same synchronizing signal **20** and ID information **21** are provided in all regions as described above, a single circuit can be used to perform the process for the generation of blocks and the detection of synchronizing signal and ID information at the time of recording. The synchronizing signal **20** may take a different value in each region so that the areas can be distinguished by only the synchronizing signal.

FIG. **5** illustrates the format of ID information **21**. There are shown a sequence number **24**, a track address **25**, a block address **26** within one track, and a parity **27** for detecting error in the sequence number **24**, track address **25** and block address **26**. The block address **26** is used to identify the block in each recording area. For example, the address is 0–335 in the data recording area **7**, 0–15 in the auxiliary information recording area **3**, and 0–15 in the subcode recording area **12**. The track address **25** is used to identify the track. For example, the address can be changed to be 0–5 or 0–2 at each track or each two tracks, thereby discriminating 6 tracks. The sequence number **24** can be changed to be 0–11 at each 6 tracks that are discriminated by the track address **25**, thereby discriminating 72 tracks. If the track address and the sequence number are respectively synchronized with the period of the second error correction code and the variable speed playback data recording period which will be described later, it is possible to make it easy to process at the recording time and discriminate at the reproducing time.

FIG. **6** illustrates the format of one-track data in the data recording area **7**. The synchronizing signal **20** and ID information **21** are omitted. The data recording area **7** is formed of, for example, 336 blocks, of which the first 306 blocks record data **41**, and of which the second 30 blocks record second error correction codes (C2 parity) **43**.

The C2 parity **43** are provided such that 10 blocks of C2 parity are added to 102 blocks of data which correspond to a fraction ⅓ of data of 306 blocks×6 tracks at each 6 tracks. The error correction code may be, for example, a Reed-Solomon code.

Data of 99 bytes of each block is formed of a header **44** of 3 bytes and data **41** of 96 bytes. FIG. **7** shows the format of the header **44** of the data recording area **7**. The header **44** is formed of format information **31**, auxiliary information **32** and block information **33**.

FIG. **8** shows the format of the format information **31**. The format information **31** is the information about recording format, and is formed of, for example, 6 bytes of 12 blocks. This information is recorded a plurality of times in a multiplex manner to improve the detection ability at the reproduction time. Data of 6 blocks includes, for example, one-block size, the number of programs being recorded, revolution rate of rotating heads, error correction code system, recording mode, format of data being recorded, and so on.

The recording mode (ID1) specifies, for example, the maximum recording capacity. In this embodiment, data of about 25 Mbps can be recorded by use of four rotating heads at a revolution rate of 1800 rpm on two channels. Here, if recording is performed on every other track, the recording capacity is about 12.5 Mbps. If recording is performed on every fourth track, the recording capacity is about 6.25 Mbps. In this case, if the tape transport speed is reduced to ½ or ¼ the original rate, the track pattern on the tape is substantially the same as the original one. Similarly, the maximum recording capacity can be decreased to 1/n the capacity of 25 Mbps. At the time of recording, the transmission rate of data being recorded is detected, and an optimum recording mode is fixed according thereto. Then, the recording mode is written in the format information **31**. For example, "1" is written for 25 Mbps, "2" for 12.5 Mbps, and "3" for 6.25 Mbps.

The format (ID2) of data being recorded specifies, for example, the length of each packet to be recorded. The amount of data to be recorded on each track is controlled in packet units, and the number of packets recorded is stored, in order that data can be transferred at an arbitrary transmission rate. The control can be made once for each track or each plurality of tracks. In addition, by storing the packet length, it is possible to treat a packet of an arbitrary length.

At the reproduction time, the format information **31** is detected so that the associated recording mode or the like is discriminated from the others, and the reproducing processor circuit is set to that mode.

FIG. **9** shows the format of the auxiliary information **32**. The auxiliary information **32** is formed of, for example, 6 blocks of 6 bytes, including an item code of the first bit indicative of the kind of information, and data of the remaining five bytes. Thus, various types of data can be recorded. For example, information of recording time or the like and kinds of recording signals are written as the auxiliary information. Also, detailed information about variable speed playback data may be included in this information in association with the format information **31**.

FIG. **10** illustrates the format of blocks of a digital compressed video signal that is transmitted in a packet form of 188 bytes and stored in the data recording area **41**. In this case, since a time stamp **25** of 4 bytes is added to the packet data, a total of 192 bytes per packet is recorded over two blocks. Since each packet of data is recorded as two blocks, namely in association with one code system of C1, error can be prevented from occurring over a plurality of packets as transmission units when each block cannot be corrected because of burst error due to dropout or the like on the tape.

FIG. **11** shows the format of blocks of packets **71** of which the length is 140 bytes. In this case, two packets **71** are recorded over three blocks. If there is only one packet, the packet is recorded over two blocks as shown in FIG. **12**. In other words, one packet is recorded over 1.5 blocks and dummy data is placed on the remaining 0.5 block

FIG. **13** shows another format of the packet given in FIG. **10**, **11** or **12**. The packet consists of, for example, time stamp **25** of 3 bytes, packet information **72** of 1 byte associated with the packet, and packet data **71** of 188 bytes or 140 bytes. If the amount of packet data **71** is less than that value, for example, 130 bytes, dummy data is added or the packet control information region may be expanded.

The time stamp **25** is information of the time in which the packet is transmitted. That is, the time at which the packet (its head) is transmitted or the interval between packets is counted on a reference clock, the count is recorded together with packet data, and the interval between packets is fixed on the basis of that information at the playback time, so that data can be produced in the same form as when transmitted.

Thus, if the ratio between the byte number of one packet and the byte number of the recording area of one block is expressed in an integral ratio n:m so that m packets can be recorded over n blocks, data can be efficiently recorded even when the packet length is different from that of the recording

area of one block. In addition, even when the number of packets is not just an integer m, for example, m'(m'<m), the m' packets can be effectively recorded by arranging over m'×n/m blocks.

The values of n and m are respectively smaller than the number of bytes of one packet and the number of bytes of the recording area of one block. Thus, the process can be easily performed by selecting integers of 10 or below for those values. Even when the length of one packet is longer than that of the recording area of one block (n>m), data can be recorded similarly. Moreover, even if the packets have different lengths, the recording and reproduction process can be performed with ease by employing the same format for the time stamp or the like. The different lengths of packets can be discriminated by use of the format information **31**.

FIG. **14** illustrates the format of block information **33**. The block information **33** is the information for discrimination of data of block units. The data information **74** is for discrimination of the kind of data recorded in the block. For example, it is turned 0 for the block in which normal packet data is recorded, 1 for the block in which no effective data is recorded, and 2 for the block in which variable speed playback data is recorded.

The block number 75 is the information for discrimination of the order of blocks when the packet data is recorded over two blocks or three blocks. For example, the block number is 0~1 when the packet data is recorded over two blocks, and 0~2 when it is recorded over three blocks. Moreover, if the end of the recording area can be known by this information, the process at the playback time can be performed with ease.

The recording and reproduction of digital data will be described below.

Even when digital data is recorded and reproduced, the recording and reproducing apparatus can be effectively operated by use of the same format as when the digital compressed video signal. However, for recording digital data, it is important to consider the reliability of data.

FIG. **15** shows the format of one track data in the data recording area **7** for digital data. In FIG. **15**, the addition of C3 parity **45** improves the data reliability. As to the parity structure, for example, the C1 parity **23** has the same format as in FIG. **6**, and the C2 parity **43** is constructed such that C2 parity of 10 blocks is added to each 102 blocks of ½ the 306 blocks of each track. The C3 parity **45** is formed such that C3 parity of 10 blocks is added to each 92 blocks which corresponds to a fraction of ½ the data of 276 blocks×6 tracks of each six tracks. Thus, by using the same numbers of parities C1 and C2 as in FIG. **6**, changing only the way of scattering C2 data and employing the same number of C3 parities as that of C2 parities, it is possible to use the error correction circuit common to both a digital compressed video signal and digital data. Moreover, by arranging the C3 parity **45** over each unit of 6 tracks the same as the C2 parity in FIG. **6**, it is possible to use the same memory capacity for scattering data, and the same way for memory control.

Of course, when the reliability is not so important, it is possible to use the same format as that shown in FIG. **6** for recording the digital compressed video signal.

When digital data is recorded, recording and reproduction are made for each unit of 6 tracks. Also, the digital data does not need time stamp **25**. Therefore, for example, data of 192 bytes of two blocks is recorded as one packet **71**. In this case, a maximum of 828 packets (158,976 bytes) can be recorded in six tracks. If the packet data is recorded in the order of the head and the following of each six tracks, and if information of whether effective data is recorded or not is included in the block information **33**, even a small amount of data to be recorded can be treated. Of course, it is not necessary to begin recording from the head.

In the recording of digital data, if part of the format information **31**, for example, a value different from that in the recording of the digital compressed video signal is selected as a recording mode, it can be detected at the playback time.

FIG. **16** shows the construction of the signal processing circuit **102**. There are shown a memory **400** in which data is stored, an error correction circuit **401** for adding C2 parity and C3 parity and performing error correction at the time of playback, a C1 parity generation circuit **411** for generating and adding the C1 parity, a recording circuit **412** for generating a recording signal, a reproducing circuit **413** for detecting the reproduced signal, an error correction circuit **414** for performing C1 error correction at the time of playback, a signal timing converter **410** for the conversion of the timing for the recording and reproduced signals, and a packet output control circuit **403** for controlling the operation timing.

FIG. **17** shows the construction of the interface circuit **107**. There are shown a packet detection circuit **300**, a time stamp detection circuit **301**, a packet output control circuit **302**, buffers **303**, **309**, and a time stamp control circuit **304**.

The operation of the apparatus at the time of recording and reproduction will be described with reference to FIGS. **16** and **17**.

The case where a digital compressed video signal is recorded and reproduced will be described first. To record and reproduce a digital compressed video signal, there are used only the adjacent +azimuth head (D+) and -azimuth head (D−), mounted on one side, of the rotating heads **100**.

At the time of recording, the operation timing of the recording and reproducing apparatus is controlled by the timing control circuit **109** on the basis of the rate of the recording data fed through the input/output terminal **108**. At the playback time, the apparatus operates on the basis of the clock generated from the oscillator **110**. The transmission rate of the packet entering and outgoing via the input/output terminal **108**A is assumed to be higher than the frequency of the clock generated as the time stamp. For example, the frequency of the reference clock of the time stamp is 27 MHz, and it enters and outgoes at a rate of 49.152 bps. In addition, the frequency is the same as that of the reference clock generated from the oscillator **110** of the recording and reproducing apparatus. As will be described later, the process for recording and playback can thus be easily performed.

At the recording time, data and synchronizing clocks are supplied via the input/output terminals **108**A and **108**B as shown by the timing of FIG. **18**. Reference numeral **310** represents the data shown in FIG. **13**. If it has no time stamp **25** added, the internally generated reference clock is added to each packet as the time stamp **25**.

The incoming data and synchronizing clocks are supplied to the packet detection circuit **300**, which detects the head of the packet in response to the clock fed from the timing signal generating circuit **105** via the input terminal **307**. The head of the packet can be detected by detecting the blank between the packets and deciding the head when data has come after the blank. Moreover, this packet detection circuit **300** is able to discriminate the kinds of packets and decide whether the packets are normally transmitted or not by detecting the number of data per each packet. In other words, if the detected packet of which the length is other than the speci-

fied packet length (which the apparatus can handle), it decides that the packet is not normally transmitted or that data not recordable has been transmitted, and supplies this information to the control circuit **104** by which the recording is stopped.

The packet **71** detected by the packet detection circuit **300** is supplied via the buffer **309** and through the output terminal **305**A to the input/output terminal **405** of the signal processing circuit **102**. The buffer **309** converts the transmission rate of input data into another value. In order to store data transmitted at a high rate of about 50 Mbps, a very fast memory is required as the memory **400**. On the other hand, since the average maximum recording rate of the recording and reproducing apparatus is about 25 Mbps as described above, the memory **400** is adapted to handle data of a rate corresponding to the maximum recording rate, and data is fed through the fast buffer **309** to the memory **400**, so that the storing speed of the memory can be reduced. FIG. **19** shows the input and output timing of the buffer **309**. If the storing rate of the memory **400** is selected to be 27 Mbps (3.375 bytes/sec), the ratio between the input rate and output rate of the buffer is about 1:2. In this case, even if the capacity of the buffer is around 7 packets, data of 7 packets or more can be continuously fed at a rate of 50 Mbps.

The signal processing circuit **102** causes the memory **400** to store packet data from the input/output terminal **405** so that a packet fed during the period corresponding to one track to be recorded can be recorded on one track. In addition, the block information **33** and so on are added at this time. The data stored in the memory **400** is fed to the error correction circuit **401** where the C2 parity is added, and then fed to the C1 parity generation circuit **411** where the C1 parity is added. Thereafter, it is fed to the recording circuit **412** where the synchronizing signal and so on are added. Thus, the recording signal illustrated in FIG. **2** is generated. This signal is fed to the signal timing converter **410**.

FIG. **20** shows the operation of the signal timing converter **410** at the time of recording. The signal timing converter **410** delays by one track the signal, to be recorded on the +azimuth track, of the recording signal that is fed in the order of +azimuth and −azimuth. The recording signals of +azimuth and −azimuth are simultaneously supplied via the input/output terminal **407** to the adjacent +azimuth head (+D) and −azimuth head (−D), located on one side, of the rotating heads **100**, by which they are recorded on the magnetic tape **111**. In other words, signals of two tracks are simultaneously recorded each time the rotating heads rotate once.

The control signals together with the packets are fed through the output terminal **306**A to the control circuit **104**, which then discriminates the kinds of packets and decides a recording mode. The time stamp **25** added to each packet is supplied to the time stamp detection circuit **301**.

The time stamp detection circuit **301** compares the intervals between packets that are counted on the time stamp **25** and the clock fed through the input terminal **307**. If there is a difference therebetween, the timing control circuit **109** responds to the control signal fed through the output terminal **308** to control the recording process timing and the revolution rate of the rotating heads **100** in order that the difference can be reduced to zero. If the recording process timing and the revolution rate of the rotating heads **100** are recorded in synchronism with the time stamp **25** at the time of recording, the reproduction and packet output can be controlled by the reference clock generated from the oscillator **110** of the recording and reproducing apparatus at the time of reproduction. That is, at the time of playback, the number of reproduced packets coincides with that of produced packets without a particular process for synchronization.

At the playback time, the reproduced signal from the +azimuth head (D+) and −azimuth head (D−) is fed through the input/output terminal **407** to the signal timing converter **410** of the signal processing circuit **102**. As illustrated in FIG. **21**, the signal timing converter **410** delays the reproduced signal from the −azimuth track by one track to produce a reproduced signal of which the +azimuth signal and −azimuth signal are alternately arranged in series. This reproduced signal is supplied to the reproducing circuit **413**. The reproducing circuit **413** detects the synchronizing signal and detects the data of the reproduced signal. Then, the error correction circuit **414** corrects data for error by use of C1 parity, and the corrected data is stored in the memory **400**. Thereafter, the error correction circuit **401** corrects the data for error by use of C2 parity. The corrected data is supplied through the input/output terminal **405** to the interface circuit **107**.

The output fed through the input/output terminal **405** has no error as a result of identifying the reproduced block information **33** and flags added at the error detection time, and it includes only the effective packets, or does not include such packets as found not to be correctable. Therefore, abnormal data can be prevented from being produced.

In the interface circuit **107**, the packet output control circuit **302** is controlled by the control signal that is fed from the control circuit **104** through the input terminal **306**B, and the reproduced packet data is produced in synchronism with the reference clock generated from the oscillator **110**. The packet fed to the input terminal **305**B is stored in the buffer **303** at a rate of, for example, 27 Mbps (3.375 bytes/sec). The packets in the buffer **303** are read in synchronism with the time stamp **25** and the clock fed through the input terminal **307** at a rate of, for example, 49.152 bps, so that they can be produced timely as shown in FIG. **19**, or according to the same timing as when the recording data was fed. Therefore, the signal after recording and reproduction can be processed in the same way as when the signal before recording is processed as it is, in the decoder for the digital compressed video signal and processors for processing the reproduced packets from other digital signal recording and reproducing apparatus.

The recording and reproduction of digital data will be described below. When digital data is recorded and reproduced, it is recorded and reproduced by the adjacent +azimuth head (D+) and −azimuth head (D−), arranged on one side, of the rotating heads **100**, while the data that is being recorded is reproduced at the same time as when it is recorded, by the adjacent +azimuth head (D+) and −azimuth head (D−) arranged on the other side. In other words, the reliability in recording can be assured by reproducing the recorded data immediately after recording so that the recorded data can be confirmed, or that it can be decided if the data has been correctly recorded.

At the recording time, data and synchronizing signals are supplied through the input/output terminals **108**A and **108**B according to, for example, the timing shown in FIG. **18**. When digital data is recorded, there is no need to manage the time stamp of data. Therefore, the packet data **310** may be the packet of only the data with no time stamp added, and particularly there is no need to manage the input intervals. Although not shown, the following cases are possible: if the data is found within the maximum recording capacity by

transmitting a data request signal to the digital data output apparatus, data is sequentially received from the digital data output apparatus; and If the data is found to exceed the limit, the digital data output apparatus is kept waiting for producing. Of course, data may take other forms than the packet form.

The input data and synchronizing clocks are supplied to the packet detection circuit **300**, at which the heads of packets are detected at the clock fed from the timing generating circuit **105** through the input terminal **307** in the same manner as the digital compressed video signal is treated.

The packet **71** detected by the packet detection circuit **300** is supplied through the buffer **309** and through the output **305A** to the input/output terminal **405** of the signal processing circuit **102**. Digital data is often fed in bursts. Therefore, for example, the capacity of the buffer **309** is selected to be 6 tracks or several times larger than that value, and data of six tracks collected in the buffer are supplied to the signal processing circuit **102** at a constant rate, so that digital data can be effectively recorded.

In the signal processing circuit **102**, the packet data fed via the input/output terminal **405** is stored in the memory **400** so that the packet data supplied during a period corresponding to one track to be recorded can be recorded on one track. At this time, block information **33** and so on are added. The data stored in the memory **400** is fed to the error correction circuit **401** where C3 and C2 parities are added, and then fed to the C1 parity generation circuit **411** where C1 parity is added. In addition, the recording circuit **412** adds the synchronizing signal **20** and so on to the output from the C1 parity generation circuit **411**, and generates the recording signal shown in FIG. **2**. This signal is supplied to the signal timing converter **410**, where it is converted in the same manner as in FIG. **20**. The converted signal is then supplied through the output terminal **407** to both the +azimuth head (D+) and −azimuth head (D−), arranged on one side, of the rotating heads **100** by which it is recorded on the magnetic tape **111**. In other words, signals of two tracks are recorded each time the rotating heads rotate once.

When digital data is recorded, the data recorded by the +azimuth head (D+) and −azimuth head (D−) on the other side is also simultaneously reproduced as shown in FIG. **22**. The reproduced data is converted by the signal timing converter **410** in the same manner as in FIG. **21**, and fed to the reproducing circuit **413** where the synchronizing signal is detected. Then, the error correction circuit **414** performs error detection on that signal by use of C1 parity. The result of error detection is fed through the input/output terminal **409** to the control circuit **104** where it is decided if the recording is correctly performed. If the error exceeds an allowable value, the data is again recorded on a different location.

Thus, since the error correction circuit **414** detects error by use of C1 parity even at the recording time, the reliability in recording can be assured without providing circuits for exclusive use.

Digital data is reproduced similarly as is the digital compressed video signal. That is, digital data is reproduced by the same +azimuth head (D+) and −azimuth head (D−) as used at the recording time, and fed from the +azimuth head (D+) and −azimuth head (D−) through the input/output terminal **407** of the signal processing circuit **102** to the signal timing converter **410**. In this converter, the reproduced signal from the −azimuth track is delayed one track so that +azimuth signal and −azimuth signal can be produced alternately in sequence as shown in FIG. **21**. This reproduced signal is fed to the reproducing circuit **413**. The reproducing circuit **413** detects the synchronizing signal and the data from the reproduced data. Then, the error correction circuit **414** performs error correction by use of C1 parity on the data and supplies the error corrected data to the memory **400** where it is stored. Thereafter, the error correction circuit **401** performs error correction on the data by use of C2 parity and C3 parity, and the corrected data is supplied through the input/output terminal **405** to the interface circuit **107**.

The interface circuit receives the output from the input/output terminal **405** and identifies the reproduced block information **33** and the flag added at the time of error correction. When digital data is reproduced, all data is required to be reproduced without error. Therefore, if a packet is found not to be correctable, the packet is, for example, again reproduced.

In the interface circuit **107**, the packet output control circuit **302** is controlled to be brought to the output mode in response to the control signal fed from the control circuit **104** through the input terminal **306B**, and it produces the reproduced packet data. When digital data is reproduced, there is no need to manage the time stamp. Therefore, the data from the buffer **303** is produced at a rate of a certain constant unit. For example, the capacity of the buffer is selected to be 6 tracks or several times greater than that, and data of each six tracks is produced from the buffer.

Thus, since the signal timing converter is used, data of two channels can be recorded and reproduced, and simultaneous reproduction at the recording time can be performed, by the recording and reproducing circuits on one channel

FIG. **23** shows the second embodiment of the digital signal recording and reproducing apparatus according to the invention. As illustrated in FIG. **23**, a digital signal is recorded and reproduced by three azimuth heads, or +azimuth head D1' (D+) and −azimuth head D3' (D−) mounted opposite to each other, and the second +azimuth head D2' (D+) mounted close to the −azimuth head.

FIG. **24** shows the construction of the signal processing circuit **102** of the digital signal recording and reproducing apparatus of FIG. **23**.

In this case, a digital compressed video signal and digital data can be recorded and reproduced without the signal timing converter **410** shown in FIG. **16**. The digital compressed video signal can be recorded and reproduced by the opposite +azimuth head (D+) and −azimuth head (D−). The digital data can be recorded and reproduced only by one +azimuth head as shown in FIG. **25**. At the recording time, the other +azimuth head is used to reproduce the recorded signal so that the recorded signal is confirmed, or that it is decided if the signal is correct as shown in FIG. **26**. Thus, since recording and reproduction are made by a single head, the maximum amount of data to be recorded is reduced to ½ the normal amount, but the signal timing converter can be eliminated. In this case, the recording circuit **412** and reproducing circuit **413** are controlled to operate only during the period of ½ the full revolution of the rotating heads.

FIG. **27** shows an example of the connection between the digital signal recording and reproducing apparatus of FIG. **1** and a digital broadcast receiver. Reference numeral **200** represents the digital signal recording and reproducing apparatus of FIG. **1**, **201** the digital broadcast receiver, **202** an antenna, and **207** a monitor, or display. In addition, reference numeral **203** designates a tuner, **204** a de-multiplex circuit, **205** a decoder, and **206** an interface circuit. A digital

broadcast signal received by the antenna **202** is demodulated by the tuner **203**, and then fed to the de-multiplex circuit **204** where a necessary digital compressed video signal is selected. The selected digital compressed video signal is decoded into a normal video signal by the decoder **205**. The output from the decoder is fed to the monitor **207**. When the received signal is a scrambled signal or other processed signal, the decoding circuit **205** descrambles and then decodes it.

The digital broadcast receiver **201** normally demodulates the received signal into the digital compressed signal, decodes the digital compressed signal into a normal video signal and audio signal by the decoder, and supplies them to the monitor of a television set. This digital compressed signal is transmitted in the normal packet form. The rate of transmission of packets is changed by the contents of a broadcast. The transmission interval of packets is also changed according to the process that was made at the encoding time. In the decoder, the frame frequency at the time of encoding is reproduced on the basis of the information included in the packet data and the interval between the transmitted packets, and the digital compressed signal is decoded into the video signal.

Before the received signal from the digital broadcast receiver **201** is recorded by the digital signal recording and reproducing apparatus, the interface circuit **206** adds a time stamp indicative of the transmission interval of packets to the digital compressed signal of the packet type and converts it into the form shown in FIG. **16**. The converted signal is fed through the input/output terminal **108** to the digital signal recording and reproducing apparatus **200**. When the time stamp is not added to the converted signal, the recording and reproducing apparatus **200** adds time information to the signal, and records it.

The digital compressed video signal reproduced by the digital signal recording and reproducing apparatus **200** is supplied from the input/output terminal **108** to the interface circuit **206** at the same intervals as at the recording time on the basis of the time stamp. The interface circuit **206** performs the same process as at the normal receiving time on the input signal, and supplies the processed signal to the decoding circuit **205**. The decoding circuit decodes it into a video signal and audio signal and supplies those signals to the monitor **207**.

FIG. **28** shows an example of the connection between the digital signal recording and reproducing apparatus of FIG. **1** and a computer. In FIG. **28**, the computer **208** is also assumed to have the function to receive the signal from the digital broadcast receiver **201**. In other words, the digital compressed signal received by the digital broadcast receiver **201** is decoded by the decoding circuit **205** incorporated in the computer **208**. The decoded signal is fed to the monitor **207**.

When a digital compressed video signal is recorded by the digital signal recording and reproducing apparatus **200**, the digital compressed video signal from the digital broadcast receiver **201** is supplied through the computer **208** to the digital signal recording and reproducing apparatus **200**. In addition, the reproduced digital compressed video signal from the apparatus **200** is decoded by the decoding circuit of the computer **208**, and then fed to the monitor **207**.

When the digital data recorded on a disk **209** or the like is recorded on the apparatus, the data recorded on the computer **208** is supplied to the apparatus **200**. The digital data reproduced from the apparatus **200** is fed to the computer **208** and recorded on the disk **209** or the like.

The interface circuit in FIG. **17** can also be used for those of other apparatus such as the digital broadcast receiver **201**.

Although the terminals for both input and output are used as input/output terminals in the above embodiments, input terminals and output terminals may be independently used.

According to the invention, since a signal timing converter is only added to the recording and reproducing circuits on one channel, the recorded data can be confirmed by simultaneous playback at the recording time without increasing the circuit scale of the apparatus for recording and reproducing the normal digital compressed video signal. Moreover, when digital data that needs high reliability is recorded and reproduced, only one azimuth head is used, and thus the number of heads can be reduced, and the signal timing converter is not necessary.

In addition, when a normal digital signal such as a digital compressed video signal is recorded and reproduced, two correction codes of C1 and C2 are used. When digital data that requires high reliability is recorded and reproduced, three correction codes of C1, C2 and C3 are used. Therefore, the recording capacity can be increased when the normal digital signal is recorded and reproduced, and reliability can be improved when digital data is recorded and reproduced. Since the correction code C2 is added to each six tracks even in the recording and reproduction of a normal digital signal, high reliability can be achieved against the dropout on the tape. Moreover, if the correction code C3 at the time of recording digital data is similarly added to each six tracks, and if the parity number is the same, the error correction circuit and memory can be used common to both cases.

What is claimed is:

1. A digital signal recording method for recording on each of tracks, or digital signal recording areas, of a magnetic recording medium a plurality of blocks each consisting of a digital signal, and added signals of a synchronizing signal, a control signal and an error correction code, said method comprising:

a first recording mode for adding a first error correction code to each n tracks (n is an integer larger than 1) of said digital signal, adding a second error correction code to each block of said digital signal and said first error correction code, and recording said digital signal with said first and second error correction codes added; and

a second recording mode for adding a third error correction code to each n tracks of said digital signal, adding a fourth error correction code to each track of said digital signal and said third error correction code, adding a second error correction code to each block of said digital signal, said third error correction code and said fourth error correction code, and recording said digital signal with said second, third and fourth error correction codes added.

2. A digital signal recording method according to claim **1**, wherein said first error correction code and said fourth error correction code have the same parity number.

3. A digital signal recording method according to claim **1**, wherein said third error correction code and said fourth error correction code have the same parity number.

4. A digital signal recording method according to claim **1**, wherein said n tracks is 6 tracks.

5. A digital signal recording method according to claim **1**, wherein said control signal includes information for discriminating between said first recording mode and said second recording mode.

6. A digital signal recording apparatus for recording on each of tracks, or digital signal recording areas, of a mag-

netic recording medium a plurality of blocks each consisting of a digital signal, and added signals of a synchronizing signal, a control signal, and an error correction code, said apparatus comprising:

a first error correction code adder which, in a first recording mode, adds a first error correction code to each n tracks (n is an integer larger than 1) of said digital signal, and which, in a second recording mode, adds a third error correction code to each n tracks of said digital signal and adds a fourth error correction code to each track of said digital signal and said third error correction code; and

a second error correction code adder which adds a second error correction code to each block of said digital signal and said first error correction code or said third error correction code and said fourth error correction code.

7. A digital signal recording apparatus according to claim 6, wherein said first error correction code and said fourth error correction code have the same parity number.

8. A digital signal recording apparatus according to claim 6, wherein said third error correction code and said fourth error correction code have the same parity number.

9. A digital signal recording and reproducing apparatus for recording on and reproducing from each of a plurality of tracks, or digital signal recording areas, of a magnetic recording medium a plurality of blocks each consisting of a digital signal having added thereto a synchronizing signal, a control signal, and an error correction code, the apparatus comprising:

a memory for storing a digital signal received for recording during a recording operation and reproduced during a reproducing operation;

an error correction code adding circuit for adding an error correction code to the digital signal stored in the memory;

a recording circuit for generating a recording signal including a plurality of blocks from the digital signal having the error correction code added thereto by the error correction code adding circuit;

a reproducing circuit for detecting the digital signal and the error correction code added thereto from a reproduced signal;

an error correction circuit for detecting and correcting errors in the digital signal detected by the reproducing circuit based on the error correction code detected by the reproducing circuit; and

a first head and a second head provided on a single rotary head assembly for recording and reproducing and arranged at opposite positions with respect to one another;

wherein during the recording operation, the recording signal generated by the recording circuit is recorded on the magnetic recording medium by the first head of the single rotary head assembly, and the recording signal recorded on the magnetic recording medium by the first head is reproduced from the magnetic recording medium by the second head of the single rotary head assembly which is opposite the first head during a period during the recording operation when the first head is not recording the recording signal on the magnetic recording medium so that the reproducing circuit and the error correction circuit can detect any error in the recording signal reproduced from the magnetic recording medium by the second head; and

wherein during the reproducing operation, the recording signal recorded on the magnetic recording medium by the first head is reproduced from the magnetic recording medium by the first head and is supplied to the memory after being subjected to error detection by the reproducing circuit and the error correction circuit.

10. A digital signal recording and reproducing apparatus according to claim **9**, wherein a first recording and reproducing mode is provided for recording by the first head during the recording operation, and for reproducing by the second head during the recording operation at the same time as recording by the first head; and

wherein a second recording and reproducing mode is provided in which reproducing is not performed by the second head.

11. A digital signal recording and reproducing apparatus according to claim **10**, wherein a third recording and reproducing mode is provided for recording and reproducing an analog signal with a third head of the single rotary head assembly.

12. A digital signal recording and reproducing apparatus according to claim **9**, wherein the first head includes two first head members having different azimuths mounted close to each other, and the second head includes two second head members having different azimuths mounted close to each other but opposing the two first head members.

13. A digital signal recording and reproducing apparatus according to claim **12**, further comprising a signal timing converter which, during the recording operation, converts the recording signal generated by the recording circuit into a signal that is supplied to the two first head members during a period corresponding to ½ a full revolution of the single rotary head assembly, and during the reproducing operation, converts the reproduced signal from the two first or two second head members during the period corresponding to ½ the full revolution of the single rotary head assembly into a sequential signal that is supplied to the reproducing circuit.

14. A digital signal recording and reproducing apparatus according to claim **9**, wherein the first head is a single first head, and the second head which opposes the first head has an azimuth which is the same as an azimuth of the first head.

15. A digital signal recording and reproducing apparatus according to claim **14**, wherein the single rotary head assembly includes a third head mounted close to the second head and having a different azimuth from the azimuths of the first head and the second head.

16. A digital signal recording apparatus for recording on each of a plurality of tracks, or digital signal recording areas, of a magnetic recording medium a plurality of blocks each consisting of a digital signal having added thereto a synchronizing signal, a control signal, and an error correction code, the apparatus comprising

a first error detection and correction adder which, in a first recording mode, adds an error detection and correction code to each n tracks (n is an integer larger than 1) of the digital signal, and which, in a second recording mode, adds the error detection and correction code to each n tracks of the digital signal and adds the error detection and correction code to each track of the digital signal; and

a second error detection and correction adder which adds the error detection and correction code to each block of the digital signal and the error detection and correction code.

* * * * *

US006792000B1

(12) **United States Patent**
Morinaga et al.

(10) **Patent No.: US 6,792,000 B1**
(45) **Date of Patent: Sep. 14, 2004**

(54) **DATA PROCESSING APPARATUS AND DATA PROCESSING METHOD, AND RECORDING MEDIUM**

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(73) Assignee: **Sony Corporation**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 697 days.

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(22) Filed: **Sep. 26, 2000**

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(52) **U.S. Cl.** **370/473**; 370/537; 386/124

(58) **Field of Search** 370/465, 473, 370/522, 527–529, 535; 386/92–98, 124

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Primary Examiner—Hassan Kizou
Assistant Examiner—Gregory B Sefcheck
(74) *Attorney, Agent, or Firm*—Frommer Lawrence & Haug LLP; William S. Frommer; Samuel H. Megerditchian

(57) **ABSTRACT**

A transport stream (TS) is recorded and the recorded TS is reproduced simultaneously. An input PID parser extracts the first packet only to be recorded, the second packet to be recorded and to be used for controlling, and the third packet to be used only for controlling from among the TS packet that constitutes the TS supplied from a descrambler. The first and second packets are supplied to a receiver and supplied to a hard disk drive (HDD) for recording. The second and third packets are supplied to an MUX. On the other hand, the TS packet stored in the HDD is read out and supplied to the MUX by way of an output PID parser. The MUX multiplexes the second or third packet supplied from the input PID parser and the TS packet read out from the HDD, and supplies the multiplexed packet to a CPU that controls a descrambler or the like.

16 Claims, 9 Drawing Sheets

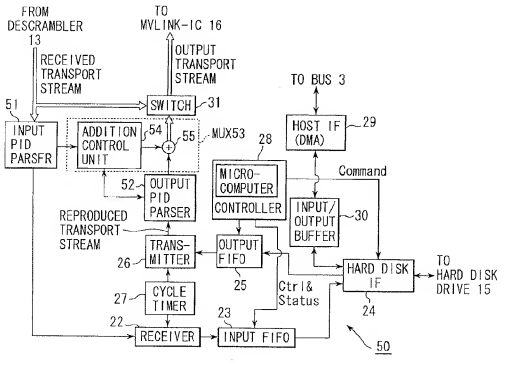
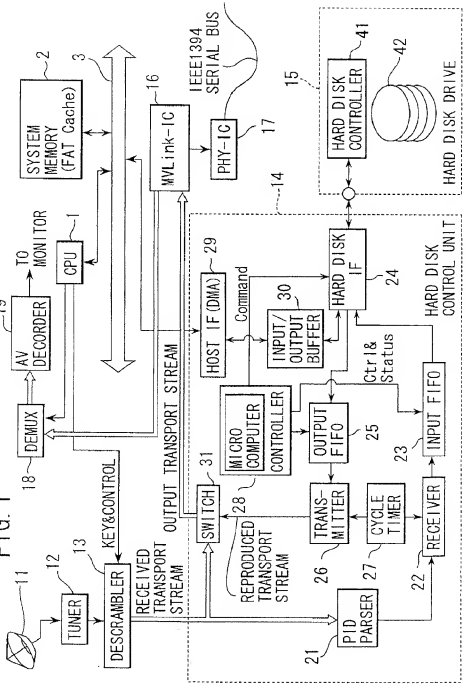


FIG. 1


11
12
TUNER
13
DESCRAMBLER
KEY&CONTROL
RECEIVED TRANSPORT STREAM
18
DEMUX
19
AV DECODER
TO MONITOR
CPU
1
SYSTEM MEMORY (FAT Cache)
2
3
16
MVLink-IC
IEEE1394 SERIAL BUS
PHY-IC
17
15
HARD DISK CONTROLLER
41
42
HARD DISK DRIVE
14
OUTPUT TRANSPORT STREAM
SWITCH
31
28
REPRODUCED TRANSPORT STREAM
MICRO COMPUTER CONTROLLER
HOST I/F (DMA)
29
Command
INPUT/ OUTPUT BUFFER
30
HARD DISK I/F
24
Ctrl & Status
TRANS-MITTER
26
OUTPUT FIFO
25
INPUT FIFO
23
CYCLE TIMER
27
RECEIVER
22
PID PARSER
21
HARD DISK CONTROL UNIT

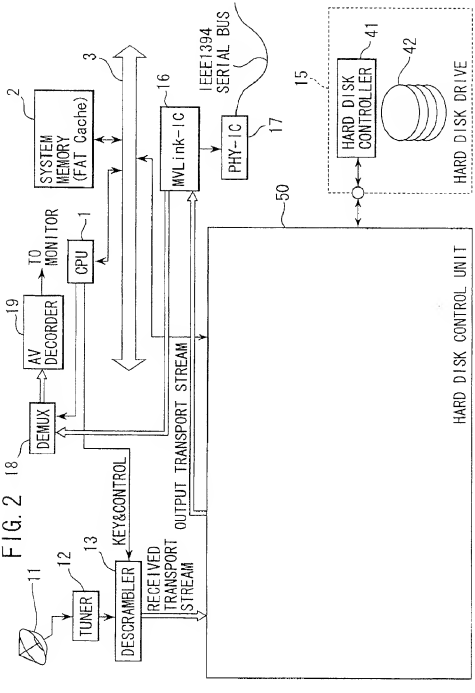

11
12
TUNER
13
DESCRAMBLER
KEY&CONTROL
RECEIVED TRANSPORT STREAM
18
DEMUX
19
AV DECORDER
TO MONITOR
CPU
1
2
SYSTEM MEMORY (FAT Cache)
3
OUTPUT TRANSPORT STREAM
16
MVLink-IC
IEEE1394 SERIAL BUS
PHY-IC
17
15
HARD DISK CONTROLLER
41
42
HARD DISK DRIVE
50
HARD DISK CONTROL UNIT

FIG. 2

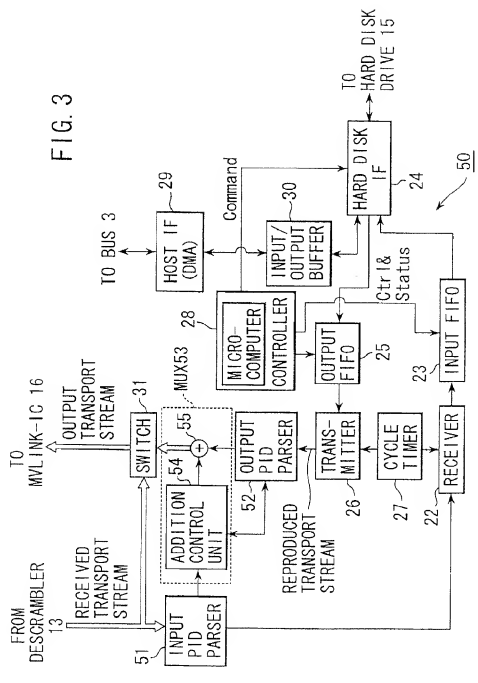

FROM DESCRAMBLER 13
RECEIVED TRANSPORT STREAM
TO MVLINK-IC 16
OUTPUT TRANSPORT STREAM
TO BUS 3
HOST IF (DMA)
29
Command
INPUT/ OUTPUT BUFFER
30
TO HARD DISK DRIVE 15
HARD DISK IF
24
50
SWITCH
31
MUX53
55
54
51
INPUT PID PARSER
ADDITION CONTROL UNIT
OUTPUT PID PARSER
52
MICRO-COMPUTER CONTROLLER
28
OUTPUT FIFO
25
Ctrl & Status
23
INPUT FIFO
REPRODUCED TRANSPORT STREAM
TRANS-MITTER
26
CYCLE TIMER
27
22
RECEIVER

FIG. 3

FIG. 4A

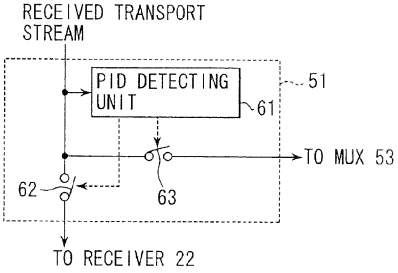


FIG. 4B

PACKET TYPE	SWITCH 62	SWITCH 63
DISCARDING PACKET	OFF	OFF
RECORDING PACKET	ON	OFF
RECORDING/CONTROLLING PACKET	ON	ON
CONTROLLING PACKET	OFF	ON

FIG. 5A

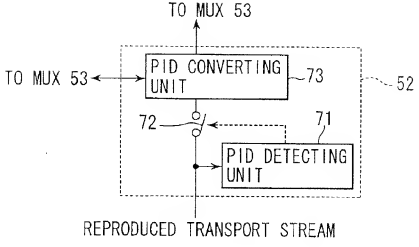


FIG. 5B

PACKET TYPE	SWITCH 72
DISCARDING PACKET	OFF
REPRODUCING PACKET	ON

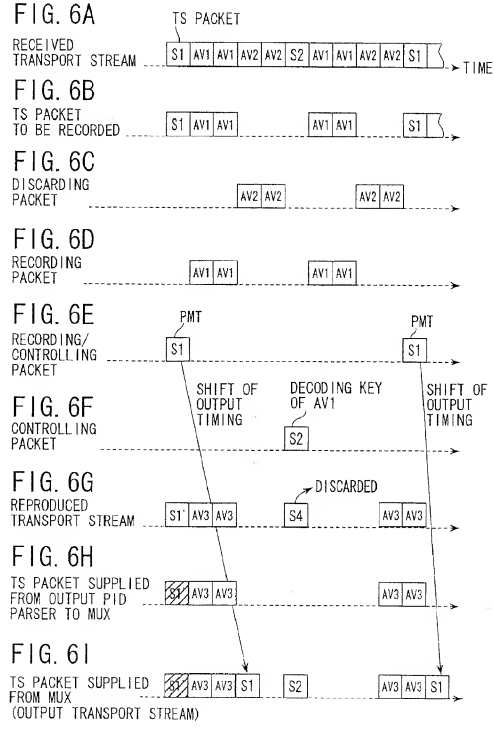


FIG. 6A
TS PACKET
RECEIVED TRANSPORT STREAM
S1 AV1 AV1 AV2 AV2 S2 AV1 AV1 AV2 AV2 S1
TIME
FIG. 6B
TS PACKET TO BE RECORDED
S1 AV1 AV1 AV1 AV1 S1
FIG. 6C
DISCARDING PACKET
AV2 AV2 AV2 AV2
FIG. 6D
RECORDING PACKET
AV1 AV1 AV1 AV1
FIG. 6E
RECORDING/ CONTROLLING PACKET
PMT
S1
PMT
S1
FIG. 6F
CONTROLLING PACKET
SHIFT OF OUTPUT TIMING
DECODING KEY OF AV1
S2
SHIFT OF OUTPUT TIMING
FIG. 6G
REPRODUCED TRANSPORT STREAM
DISCARDED
S1 AV3 AV3
S4
AV3 AV3
FIG. 6H
TS PACKET SUPPLIED FROM OUTPUT PID PARSER TO MUX
S1 AV3 AV3
AV3 AV3
FIG. 6I
TS PACKET SUPPLIED FROM MUX (OUTPUT TRANSPORT STREAM)
S1 AV3 AV3 S1
S2
AV3 AV3 S1

FIG. 7

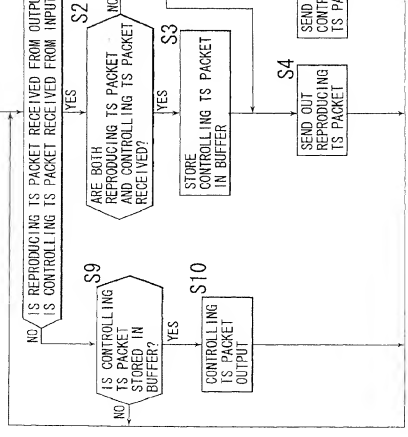

MULTIPLEXING PROCESSING
S1
IS REPRODUCING TS PACKET RECEIVED FROM OUTPUT PID PARSER? IS CONTROLLING TS PACKET RECEIVED FROM INPUT PID PARSER?
NO
YES
S2
ARE BOTH REPRODUCING TS PACKET AND CONTROLLING TS PACKET RECEIVED?
NO
YES
S3
STORE CONTROLLING TS PACKET IN BUFFER
S4
SEND OUT REPRODUCING TS PACKET
S5
IS THIS REPRODUCING TS PACKET?
YES
NO
S6
IS CONTROLLING TS PACKET STORED IN BUFFER?
NO
YES
S7
STORE RECEIVED CONTROLLING TS PACKET IN BUFFER, AND SEND OUT STORED CONTROLLING TS PACKET
S8
SEND OUT CONTROLLING TS PACKET
S9
IS CONTROLLING TS PACKET STORED IN BUFFER?
NO
YES
S10
CONTROLLING TS PACKET OUTPUT

FIG. 8A

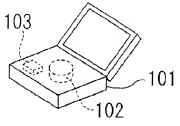


FIG. 8B

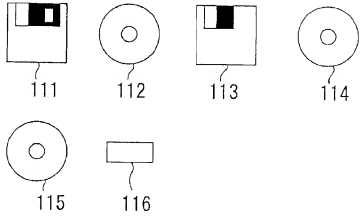


FIG. 8C

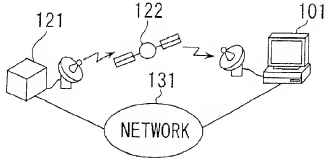
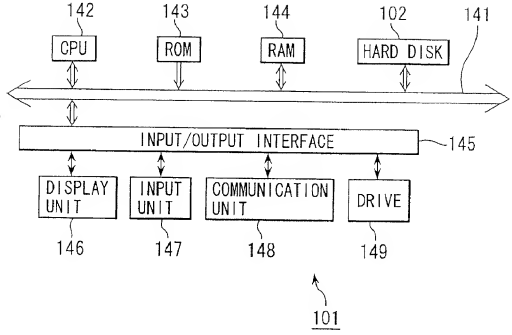


FIG. 9


142
143
144
102
141
CPU
ROM
RAM
HARD DISK
INPUT/OUTPUT INTERFACE
145
DISPLAY UNIT
INPUT UNIT
COMMUNICATION UNIT
DRIVE
146
147
148
149
101

DATA PROCESSING APPARATUS AND DATA PROCESSING METHOD, AND RECORDING MEDIUM

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a data processing apparatus and a data processing method, and a recording medium, and more particularly relates to a data processing apparatus and a data processing method, and a recording medium that are capable of simultaneous recording and reproducing of a digital satellite broadcast program.

2. Description of Related Art

Recently, the digital satellite broadcasting has been started practically, and various digital satellite broadcast receiving apparatus have been commercialized.

However, no digital satellite broadcast receiving apparatus having a built-in storage device such as a hard disk or the like for recording a digital satellite broadcast program has not yet been commercialized at present time.

Furthermore, in the commercialization of such digital satellite broadcast receiving apparatus, it would be likely needed in the future that such a digital satellite broadcast receiving apparatus is provided with a simultaneous recording and reproducing function like so-called delayed playback that is a function for reproducing a digital satellite broadcast program recorded in a storage device while the received digital satellite broadcast program is being recorded in the storage device.

SUMMARY OF THE INVENTION

The present invention has been accomplished in view of the above, for example, the digital data such as the recorded digital satellite program or the like is reproduced while the digital data is being recorded by applying the present invention.

A data processing apparatus of the present invention comprises packet extracting means at least for extracting a first packet only to be recorded, a second packet to be recorded and to be used for controlling, and a third packet to be used only for controlling from among component packets of the received stream, packet output means for supplying the first and second packets to a recording unit for recording the data, and multiplexing means for multiplexing the second and third packets and a packet reproduced from the recording unit and for sending out the multiplexed packet.

The stream composed of packets of the predetermined format may be a transport stream. In this case, converting means, that converts the PID of any one of the second or third packet and the packet reproduced from the recording unit in the case that the PID (Packet Identification) of the second or third packet is identical with the PID of the packet reproduced from the recording unit, is additionally provided.

When the multiplexing means receives the second or third packet and the packet reproduced from the recording unit simultaneously, the multiplexing means temporarily stores the second or third packet and sends out the packet reproduced from the recording unit, and sends out the stored second or third packet when the packet reproduced from the recording unit is not received.

A recording unit may be provided additionally.

A data processing method of the present invention comprises a packet extracting step at least for extracting the first packet only to be recorded, a second packet to be recorded and to be used for controlling, and a third packet to be used only for controlling from among component packets of the received stream, a packet output step of supplying the first and second packets to a recording unit for recording the data, and a multiplexing step of multiplexing the second and third packets and a packet reproduced from the recording unit and for sending out the multiplexed packet.

A recording medium of the present invention characterized by containing a recorded program comprises a packet extracting step at least of extracting a first packet only to be recorded, a second packet to be recorded and to be used for controlling, and a third packet to be used only for controlling from among component packets of the received stream, a packet output step of supplying the first and second packets to a recording unit for recording the data, and a multiplexing step of multiplexing the second and third packets and a packet reproduced from the recording unit and for sending out the multiplexed packet.

In the data processing apparatus and the data processing method, and the recording medium of the present invention, at least a first packet only to be recorded, a second packet to be recorded and to be used for controlling, and a third packet to be used only for controlling are extracted from among packets that constitute the received stream. The first and second packets are supplied to the recording unit for recording the data, and the second and third packets and a packet reproduced from the recording unit are multiplexed and sent out.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram for illustrating an exemplary structure of a digital satellite broadcast receiving apparatus having a built-in hard disk drive **15**.

FIG. **2** is a block diagram for illustrating an exemplary structure of one embodiment of a digital satellite broadcast receiving apparatus to which the present invention is applied.

FIG. **3** is a block diagram for illustrating an exemplary structure of a hard disk control unit **50** shown in FIG. **2**.

FIG. **4**A and FIG. **4**B are diagrams for describing the detail of an input PID parser **51** shown in FIG. **3**.

FIG. **5**A and FIG. **5**B are diagrams for describing the detail of an output PID parser **52** shown in FIG. **3**.

FIG. **6**A to FIG. **6**I are time charts for describing the processing performed when the transport stream is recorded and reproduced simultaneously in the digital satellite broadcast receiving apparatus shown in FIG. **2**.

FIG. **7** is a flow chart for describing the processing of an MUX **53** shown in FIG. **3**.

FIG. **8**A to FIG. **8**c are diagrams for describing a recording medium to which the present invention is applied.

FIG. **9** is a block diagram for illustrating an exemplary structure of a computer **101** shown in FIG. **8**A.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **1** shows an exemplary structure of a digital satellite broadcast receiving apparatus having a built-in hard disk drive **15** served as a storage device for receiving the digital satellite broadcast.

The digital satellite broadcast receiving apparatus receives a transport stream as the digital satellite broadcast program from a broadcasting station not shown in the

drawing and displays the image and sound as the transport stream thereof, and furthermore reproduces the recorded transport stream that has been recorded.

In detail, an antenna **11** receives the digital satellite broadcast wave, and the received signal is supplied to a tuner **12**. The tuner **12** decodes the signal received from the antenna **11** to obtain the transport stream, and supplies it to a descrambler **13**. The descrambler **13** descrambles the scrambled transport stream supplied from the tuner **12** by use of a decoding key supplied from a CPU **1** under the control by means of the CPU **1**, and supplies it to a hard disk control unit **14**.

The transport stream supplied from the descrambler **13** (referred to as received transport stream hereinafter properly) is supplied to a PID (Packet Identification) parser **21** and a switch **31**. In addition to the received transport stream, the transport stream reproduced by means of the hard disk drive **15** is supplied to the switch **31** by way of a transmitter **26**.

When the received transport stream is to be reproduced, the switch **31** selects the received transport stream from among two transports supplied thereto (the received transport stream and the transport stream supplied from the transmitter **26**), and supplies it to an MVLink-IC (MVLink-IC (MPEG (Moving Picture Experts Group) Link Integrated Circuit) **16**.

The MVLink-IC **16** subjects the link layer processing in the layer structure of IEEE (Institute of Electrical and Electronics Engineers) 1394 serial bus to the output transport stream, and supplies it to a PHY-IC **17**. Otherwise, the MVLink-IC **16** supplies the output transport stream to a DEMUX (demultiplexer) **18**.

Herein, the PHY-IC **17** performs the link layer processing in the layer structure of the IEEE 1394 serial bus, and when the PHY-IC **17** receives the output transport stream from the MVLink-IC **16**, the PHY-IC **17** isochronously transfers the output transport stream to an IEEE 1394 apparatus not shown in the drawing by way of the IEEE 1394 serial bus.

The DEMUX **18**, having a microcomputer and memory or the like that are not shown in the drawing, separates the TS packet on which the section data (the control data used for controlling the decoding key for descrambling the scrambled PAT (Program Association Table), PMT (Program Map Table), and transport stream and others) are loaded from the transport packet that constitutes the output transport stream (referred to as TS packet hereinafter properly) supplied from the MVLink-IC **16**, and furthermore analyzes the content thereof, and supplies the necessary control data to the CPU **1**.

As described hereinabove, the CPU1 supplies the decoding key out of the section key supplied from the DEMUX **18** to the descrambler **13**, and controls the descrambler **13** based on other section data supplied from the DEMUX **18**.

The DEMUX **18** not only separates the TS packet on which the control data is loaded from the output transport stream but also separates the packet on which the video data and the audio data (referred to as AV data including both data hereinafter properly) of the selected program are loaded, and the DEMUX **18** supplies the AV data to an AV decoder **19**.

The AV decoder **19** MPEG (Moving Picture Experts Group) 2-decodes the TS packet supplied from the DEMUX **18**, and supplies the resultant AV data to a monitor not shown in the drawing. Thereby, the image and sound of the digital satellite broadcast program are reproduced (displayed) on the monitor.

On the other hand, in the case that the received transport stream is to be recorded, the switch **31** also selects the received transport stream from among two input transport streams (the received transport stream and the transport stream supplied from the transmitter **26**), and supplies it to the DEMUX **18** by way of the MVLink-IC **16** as the output transport stream.

As described hereinabove, the DEMUX **18** separates the TS packet on which the control data is loaded from the output transport stream, then separates the necessary data loaded on the TS, and supplies it to the CPU **1**. The CPU **1** controls the descrambler **13** based on the control data. Thereby, the descrambler **13** descrambles the transport stream containing the TS packet that is to be recorded.

The received transport stream is also supplied to the PID parser **21** as described hereinabove, and the PID parser **21** supplies only the TS packet of the program that is to be recorded to a receiver **22** with reference to the PID of the TS packet that constitutes the received transport stream supplied thereto (residual TS packet is discarded). The receiver **22** adds the time stamp based on the clock generated by means of the cycle timer **27** to the TS packet supplied from the PID parser **21**, and supplies it to an input FIFO (First In First Out) **23**. In other words, the cycle timer **27** supplies the clock having a predetermined frequency to the receiver **22** and transmitter **26**, and the receiver **22** adds the time stamp that is synchronous with the clock generated by means of the cycle timer **27** to the TS packet supplied from the PID parser **21** and supplies it to the input FIFO **23**. The input FIFO **23** stores the TS packet supplied from the receiver successively, and supplies the stored TS packet in FIFO-fashion to a hard disk IF (Interface) **24** according to the control by means of a controller **28**.

The controller **28** having a built-in microcomputer monitors the storage status in the input FIFO **23** or an output FIFO **25**, and controls data reading/writing in the input FIFO **23** and the output FIFO **25**. Furthermore, the controller **28** controls the hard disk IF **24**.

Upon receiving the TS packet from input-FIFO **23**, the hard disk IF **24** supplies the TS packet to the hard disk drive **15**.

In the hard disk drive **15**, the TS packet is received by means of a hard disk controller **41** and recorded in a hard disk **42**.

Next, in the case that the TS packet recorded in the hard disk **42** as described hereinabove is to be reproduced, the hard disk controller **41** reads out the transport stream that is served as the sequence of the TS packet recorded in the hard disk **42** (referred to as reproduced transport stream hereinafter properly) and supplies it to the hard disk control unit **14**.

In the hard disk control unit **14**, the hard disk IF **24** receives the reproduced transport stream and supplies it to the output FIFO **25**. The output FIFO **25** stores the TS packet that constitutes there produced transport stream supplied from the hard disk IF **24** successively, and sends out the stored TS packet in the order of FIFO-fashion to the transmitter **26** according to the control by means of the controller **28**. The transmitter **26** supplies the reproduced transport stream that is served as the sequence of the TS packet supplied from the output FIFO **25** to the switch **31** synchronously with the clock supplied from the cycle timer **27**. In other words, when the transport stream that is served as the sequence of the TS packet generated by means of the PID parser **21** is recorded in the hard disk drive **15**, the time interval between TS packets that constitute the transport stream could be irregular. To solve the problem, the transmitter **26** supplies the TS packet to the switch **31** at the

timing so as to restore the time interval between TS packets to the original time interval with reference to the time stamp added to the TS packet.

When the TS packet-recorded in the hard disk **42** is reproduced, the switch **31** selects the reproduced transport stream supplied from the transmitter **26**, and supplies it to the MVLink-IC **16** as the output transport stream. Thereafter, the reproduced transport stream that is served as the output transport stream is isochronously transferred on the IEEE 1394 serial bus by way of the PHY IC **17** as in the case of processing of the received transport stream, or supplied to the monitor by way of the DEMUX **18** and decoder **19**.

The CPU **1** that is connected to the bus **3** reads out and executes the program stored in the system memory **2** that is connected to the same bus **3** to thereby control the descrambler **13** and perform various other processing. The system memory **2** stores various programs for the CPU **1** to perform various processing.

Furthermore, a host IF **29** that is a component of the hard disk control unit **14** functions as an interface for communicating with the CPU **1** by way of the bus **3**. The host IF **29** and an input/output buffer **30** provided between the host IF **29** and the above-mentioned hard disk IF **24** temporarily store the data that is communicated between them.

As described hereinabove, the CPU **1** takes an access to the had disc drive **15** by way of the bus **3**, host IF **29**, input/output buffer **30**, and hard disk IF **24**. Thereby, the CPU **1** records the data in the form of file in the hard disk drive **15** and reads out the data in the form of file recorded in the hard disk drive **15**.

The digital satellite broadcast receiving apparatus having the structure as described in FIG. **1** cannot function to perform simultaneous recording and reproducing unlike so-called delayed playback in which the received transport stream is recorded by means of the hard disk drive **15** while the recorded transport stream is being reproduced.

In other words, as described hereinabove, the switch **31** of the hard disk control unit **14** selects the received transport stream supplied from the descrambler **13** and sends it out as the output transport stream when the received transport stream is to be recorded, and on the other hand selects the reproduced transport stream supplied from the transmitter **26** and sends it out as the output transport stream when the transport stream stored in the hard disk drive **15** is to be reproduced.

Though it is required for switch **31** to select the reproduced transport stream supplied from the transmitter **26** consistently in order to reproduce the transport stream recorded in the hard disk drive **15**, in this case the switch **31** cannot select the received transport stream supplied from the descrambler **13** as an output transport stream and cannot supply it to the DEMUX **18** by way of the MVLink-IC **16**. As the result, the CPU **1** cannot obtain a decoding key used by means of the descrambler **13**, and the descrambler **13** cannot descramble the transport stream.

Furthermore, in this case, because the control data loaded on the TS packet that constitutes the received transport stream is not supplied at all to the CPU **1**, the CPU **1** cannot get the information or the like necessary for knowing the status of the digital satellite broadcast in real time, various problems likely occur.

In view of the above problem, an exemplary structure of an embodiment of a digital satellite broadcast receiving apparatus to which the present invention is applied is shown in FIG. **2**. In FIG. **2**, the components corresponding to those shown in FIG. **1** are given the same characters, and the description is omitted hereinafter. In detail, the digital satellite broadcast receiving apparatus shown in FIG. **2** has the same structure as that of the digital satellite broadcast receiving apparatus shown in FIG. **1** excepting that a hard disk control unit **50** is provided instead of the hard disk control unit **14** shown in FIG. **1**.

FIG. **3** shows an exemplary structure of the hard disk control unit **50** shown in FIG. **2**. In FIG. **3**, the same components corresponding to those of the hard disk control unit **14** shown in FIG. **1** are given the same characters, and the description is omitted hereinafter. The hard disk control unit **50** has the same structure as that of the hard disk control unit **14** shown in FIG. **1** excepting that the hard disk control unit **50** is provided additionally with an input PID parser **51**, an output PID parser **52**, and an MUX (multiplexer) **53**, and the PID parser **21** is eliminated.

The received transport stream supplied from the descrambler **13** is supplied to the switch **31** and the input PID parser **51**. From the TS packet that constitutes the received transport stream supplied from the descrambler **13**, the input PID parser **51** extracts the TS packet to be only recorded (referred to as recording packet hereinafter properly), the TS packet to be recorded and to be used for controlling (referred to as recording/controlling packet hereinafter properly), the TS packet to be used for only control (referred to as controlling packet hereinafter properly), and the TS packet to be discarded (referred to as discarding packet hereinafter properly), and supplies the recording packet and the recording/controlling packet to the receiver **22** and supplies the controlling packet to the MUX **53**. Furthermore, the input PID parser **51** discards the discarding packet.

The output PID parser **52** receives the reproduced transport stream that has been reproduced by means of the hard disk drive **15** and has been supplied from the transmitter **26**, and extracts the TS packet to be reproduced (referred to as reproducing packet hereinafter properly) and the TS packet to be discarded (discarding packet) from among the TS packets that constitute the reproduced transport stream. Furthermore, the output PID parser **52** supplies the reproducing TS packet to the MUX **53** and discards the discarding packet.

Furthermore, the output PID parser **52** communicates with an addition control unit **54**, which will be described hereinafter, of the MUX **53** to thereby detects the reproducing TS packet having the same PID as that of TS packet supplied to the MUX **53** from the input PID parser **51**, and convert the PID of the reproducing TS packet to a different PID.

The MUX **53** comprising the addition control unit **54** and a gate circuit **55** multiplexes the TS packet supplied from the input PID parser **51** and the TS packet supplied from the output PID parser **52**, and supplies them to the switch **31**. In detail, the addition control unit **54** shifts the output timing of the TS packet that the addition control unit **54** itself is going to send out when the timing of output of the TS packet from the input PID parser **51** to the gate circuit **55** coincides with the timing of output of the TS packet from the output PID parser **52** to the gate circuit **55**. Thereby, collision between the TS packet sent out from the input PID parser **51** itself and the TS packet sent out from the output PID parser **52** on the gate circuit **55** is prevented. The gate circuit **55** nicely transfers the TS packet supplied from the addition control unit **54** and the TS packet supplied from the output PID parser **52** to the switch **31**.

Next, the detail of the input PID parser **51** shown in FIG. **3** will be described with reference to FIG. **4**A and FIG **4**B.

FIG. **4**A shows an exemplary structure of the input PID parser **51**.

As shown in FIG. **4**A, the input PID parser **51** comprises a PID detecting unit **61** and switches **62** and **63**.

The PID detecting unit **61** detects the PID of the TS packet that constitutes the received transport stream supplied from the descrambler **13**, and controls the switches **62** and **63** based on the detection result.

The switch **62** is turned ON/OFF under the control by means of the PID detecting unit **61** to thereby control the supply of the TS packet that constitutes the received transport stream to the receiver **22**. The switch **63** is also turned ON/OFF under the control by means of the PID detecting unit **61** to thereby control the supply of the TS packet that constitutes the received transport stream to the MUX **53**.

The input PID parser **51** having the structure as described hereinabove supplies the TS packet that constitutes the received transport stream supplied from the descrambler **13** to the PID detecting unit **61** and the switches **62** and **63**.

The PID detecting unit **61** detects the PID of the TS packet supplied thereto and recognizes whether the TS packet is the TS packet on which the AV data to be recorded is loaded, the TS packet on which the control data necessary to reproduce the AV data is loaded, the TS packet on which the control data necessary to descramble the transport stream supplied from the tuner **12** is loaded, or the TS packet that does not correspond to any one of the above TS packets.

If the TS packet corresponds to the TS packet on which the AV data to be recorded is loaded, then the PID detecting unit **61** controls the switches **62** and **63** on the assumption that the TS packet is a recording packet. If the TS packet corresponds to the TS packet on which the control data necessary to reproduce the AV data is loaded, then the PID detecting unit **61** controls the switches **62** and **63** on the assumption that the TS packet is a recording/controlling packet. If the TS packet correspond to the TS packet on which the control data necessary to descramble the transport stream supplied from the tuner is loaded, then the PID detecting unit **61** controls the switches **62** and **63** on the assumption that the TS packet is a controlling packet. If the TS packet corresponds to the TS packet that does not corresponds to any one of the above-mentioned TS packets, then the PID detecting unit **61** controls the switches **62** and **63** on the assumption that the TS packet is a discarding packet.

In other words, the PID detecting unit **61** controls the switches **62** and **63** as shown in FIG. **4**B.

In detail, in the case that the TS packet is a discarding packet, the switches **62** and **63** are both turned OFF, and as the result the TS packet is supplies neither to the receiver nor to the MUX **53** and discarded. In the case that the TS packet is a recording packet, the switch **62** or **63** is turned ON or OFF, and as the result the TS packet is supplied only to the receiver **22**. Furthermore, in the case that the TS packet is a recording/controlling packet, the switches **62** and **63** are both turned ON, and as the result the TS packet is supplied both to the receiver **22** and the MUX **53**. Furthermore, in the case that the TS packet is a recording packet, the switch **62** or **63** is turned OFF or ON, and as the result the TS packet is supplied only to the MUX **53**.

As described hereinabove, the discarding packet is discarded, and the recording packet is recorded in the hard disk drive **15**. Furthermore, the recording/controlling packet is recorded in the hard disk drive **15** and supplied to the MUX **53**, and the controlling packet is supplied to the MUX **53**.

Next, the detail of the output PID parser **52** shown in FIG. **3** will be described with reference to FIG. **5**A and FIG. **5**B.

FIG. **5**A shows an exemplary structure of the output PID parser **52**.

As shown in FIG. **5**A, the output PID parser **52** comprises a PID detecting unit **71**, a switch **72**, and a PID converting unit **73**.

The PID detecting unit **71** detects the PID of the TS packet that constitutes the reproduced transport stream supplied from the transmitter **26** and controls the switch **72** based on the detection result like the PID detecting unit **61** shown in FIG. **4**A and FIG. **4**B.

The switch **72** is turned ON/OFF under the control by means of the PID detecting unit **71** to thereby control the supply of the TS packet that constitutes the reproduced transport stream to the PID converting unit **73**.

The PID converting unit **73** communicates with the MUX **53**, converts the PID of the TS packet to be supplied by way of the switch **72** as required, and supplies the TS packet to the MUX **53**.

The output PID parser **52** having the structure as described hereinabove supplies the TS packet that constitutes the reproduced transport stream supplied from the transmitter **26** to the PID detecting unit **71** and the switch **72**.

The PID detecting unit **71** detects the PID of the TS packet supplied thereto, and recognizes whether the TS packet is the TS packet to be reproduced or the TS packet that is not necessary to be reproduced based on the PID.

If the TS packet corresponds to the TS packet to be reproduced, then the PID detecting unit **71** controls the switch **72** on the assumption that the TS packet is a reproducing packet, on the other hand if the TS packet corresponds to the TS packet that is not necessary to be reproduced, then the PID detecting unit **71** controls the switch **72** on the assumption that the TS packet is a discarding packet.

In detail, the PID detecting unit **71** controls the switch **72** as shown in FIG. **5**B.

Therefore, if the TS packet is a discarding packet, then the switch **72** is turned OFF, and as the result the TS packet is discarded without being supplied to the PID converting unit **73**. On the other hand, if the TS packet is a reproducing packet, then the switch **72** is turned ON, and as the result the TS packet is supplied to the PID converting unit **73**.

Upon receiving the TS packet (reproducing packet) by way of the switch **72**, the PID converting unit **73** supplies the TS packet to the gate circuit **55** of the MUX **53**. However, the PID converting unit **73** communicates with the addition control unit **54** of the MUX **52**, and if the TS packet that is to be supplied to the gate circuit **55** of the MUX **52** from the PID converting unit **73** itself has the same PID as that of the TS packet that the addition control unit of the MUX **53** is going to supply to the gate circuit **55**, then the PID converting unit **73** converts the PID of the TS packet that is to be supplied from the PID converting unit **73** itself to a different PID, and supplies the TS packet having the converted PID to the gate circuit **55**.

Because the PID is converted even though it is the TS packet that is to be broadcasted in the same channel excepting the special TS packet (for example, the TS packet on which PAT is loaded), the same PID can be allocated both to the TS packet supplied from the input PID parser **61** to the

MUX **53** and the TS packet supplied from the output PID parser **52** to the MUX **53** though different data is loaded on both TS packets. In this case, the different data is loaded in the DEMUX **18**, it can be difficult to analyze the TS packet to which the same PID is allocated. To solve such problem, the PID converting unit **73** converts the PID of the TS packet that is to be sent out from the PID converting unit **73** itself to a PID different from the PID of the TS packet that is to be sent out from the addition control unit **54** if the TS packet that is to be sent out from the PID converting unit **73** itself to the gate circuit **55** of the MUX **52** is identical with the PID of the TS packet that is to be sent out from the addition control unit **54** of the MUX **53** to the gate circuit **55**.

Next, when the digital satellite broadcast receiving apparatus shown in FIG. **2** receives the transport stream served as the digital satellite broadcast program and displays the image and sound served as the transport stream, the same processing as that performed by means of the digital satellite broadcast receiving apparatus shown in FIG. **1** is performed.

In detail, the antenna **11** received the digital satellite broadcast wave, the obtained received signal is supplied to the tuner **12**, and the tuner **12** demodulates the received signal supplied from the antenna **11** to obtain the transport stream, and the transport stream is supplied to the descrambler **13**. The descrambler **13** descrambles the scrambled transport stream supplied from the tuner **12** by use of a decoding key supplied from the CPU **1**, and supplies it to the hard disk control unit **50**.

The transport stream supplied from the descrambler **13** (received transport stream) is supplied to the input PID parser **51** and the switch **31** of the hard disk control unit **50** (FIG. **3**). In this case, the switch **31** selects the received transport stream supplied from the descrambler **13**, and supplies it to the MVLink-IC **16** as the output transport stream.

Subsequently, the output transport stream is isochronously transferred on the IEEE 1394 serial bus by way of the PHY-IC **17** or supplied to the monitor by way of the DEMUX **18** and the decoder **19** as in the case shown in FIG. **1**.

In this case, because the received transport stream is supplied to the DEMUX **18** as the output transport stream, the DEMUX **18** obtains the necessary control data from the received transport stream and supplies it to the CPU **1**. Therefore, the descrambler **13** can descramble the transport stream supplied from the tuner **12**.

Next, when the received transport stream is to be recorded, the switch **31** selects the received transport stream supplied from the descrambler **13**, and supplies it to the DEMUX **18** by way of the MVLink-IC **16** as the output transport stream. Therefore, also in this case, the DEMUX **18** obtains the necessary control data from the received transport stream supplied as the output transport stream and can supply it to the CPU **1**, and as the result the descrambler **13** can descramble the transport stream supplied from the tuner **12**.

Furthermore, in this case, the input PID parser **51** supplies only the TS packet of the program that is to be recorded (the above-mentioned recording packet and the recording/controlling packet) and discards the residual TS packet with referring to the PID of the TS packet that constitutes the received transport stream supplied thereto. Subsequently the same processing as performed in the case shown in FIG. **1** is performed, and the TS packet supplied from the input PID parser **51** to the receiver **22** is recorded in the hard disk drive **15**.

Next, when the TS packet recorded in the hard disk drive **15** as described hereinabove is to be reproduced, the TS packet recorded in the hard disk drive **15** is reproduced as in the case shown in FIG. **1**, and the reproduced transport stream obtained as the result is supplied from the transmitter **26** to the output PID parser **52**.

The output PID parser **52** supplies only the TS packet to he reproduced (the above-mentioned reproducing packet) to the MUX **53** with referring to the PID of the TS packet that constitutes the reproduced transport stream supplied thereto, and discards the residual TS packet.

The MUX **53** supplies the TS packet supplied from the output PID parser **52** to the gate circuit **55**. Furthermore, in this case, because only reproduction of the TS packet recorded in the hard disk drive **15** is performed, the TS packet is not supplied from the input PID parser **51** to the gate circuit **55** by way of the addition control unit **54**. Therefore, the gate circuit **55** allows the TS packet to be supplied from the output PID parser **52** to the switch circuit **31** successively.

Subsequently, in the same manner as shown in FIG. **1**, the TS packet recorded in the hard disk drive **15** is isochronously transferred on the IEEE 1394 serial bus by way of the PHY-IC **17** or supplied to the monitor by way of the DEMUX **18** and the decoder **19**.

Next, the processing performed when the digital satellite broadcast receiving apparatus shown in FIG. **2** reproduces the transport stream recorded already in the hard disk drive **15** while the received transport stream is being recorded in the hard disk drive **15** will be described with reference to FIG. **6**.

For example, it is assumed that the transport stream composed of sequential TS packets as shown in FIG. **6**A is supplied from the descrambler **13** to the hard disk control unit **50** as the received transport stream.

In FIG. **6**A to FIG. **6**I, a square having S and a numeral represents a TS packet on which the control data is loaded, and a square having AV and a numeral represents a TS packet on which the AV data is loaded.

In the received transport stream shown in FIG. **6**A, it is assumed that the control data S1 loaded on a TS packet #S1 (a TS packet on which the data S1 is loaded) contains the information necessary for reproducing the AV data AV1 loaded on a TS packet #AV1 (for example, PMT on which PID of the TS packet #AV1 or the like), and furthermore, for example, the control data S2 loaded on a TS packet #S2 contains a decoding key for descrambling the transport stream (payload of the TS packet) in the descrambler **13**.

In this case, it is assumed that the AV data AV1 is the AV data of the program to be recorded, then it is necessary to record TS packets #S1, #AV1 shown in FIG. **6**B out of the TS packets that are components of the received transport stream shown in FIG. **6**A. In other words, it is necessary to record not only the AV data AV1 that is to be recorded but also the control data S1 that is necessary for reproducing.

Furthermore, it is necessary to supply the TS packet #S2 to the CPU **1** in order to descramble the transport stream by means of the descrambler **13**.

Accordingly, TS packets #AV2 on which the AV data AV2 is loaded is unnecessary out of the TS packets that are components of the received transport stream shown in FIG. **6**A and these TS packets is to be discarded as shown in FIG. **6**C. When the input PID parser **51** (FIG. **4**A and FIG. **4**B) receives a TS packet AV2 by means of the PID detecting unit **61**, the switches **62** and **63** are both turned OFF as described hereinabove and the TS packet AV2 is thereby discarded.

Furthermore, a TS packet #AV1 on which the AV data AV1 to be recorded is loaded is the recording packet that is only to be recorded, the switches **62** or **63** is turned ON or OFF at the timing when a TS packet is received as shown in FIG. **6**D in the PID detecting unit **61** of the input PID parser **51**, and the TS packet AV1 is thereby supplied to the receiver **22** and recorded in the hard disk driver **15**.

It is necessary to record the control data S1 such as PMT or the like loaded on a TS packet #S1 that is to be recorded because the control data S1 is necessary for reproducing the AV data AV1, and also it is necessary to supply the control data S1 to the CPU **1** in order to recognize the data loaded on the TS packet based on the PID of the TS packet by means of the DEMUX **18** or the like. Therefore, the TS packet #S1 is recorded and also served as the recording/controlling packet used by the CPU **1** for controlling. In the PID detecting unit **61** of the input PID parser **51** (shown in FIG. **4**A and FIG. 4B) the switches **62** and **63** are both turned ON at the timing when a TS packet #S1 is received as shown in FIG. **6**E, the TS packet #S1 is thereby supplied to the receiver **22** and recorded in the hard disk drive **15**, and supplied to the MUX **53** and subsequently supplied to the CPU **1** as described hereinafter.

Because the control data S2 such as a decoding key or the like loaded on a TS packet #S2 is necessary for the descrambler **13** to descramble but not necessary to reproduce the AV data AV1 to be recorded, the TS packet #S2 is the controlling packet used only for controlling. In the PID detecting unit **61** of the input PID parser **51** (FIG. **4**A and FIG. 4B), the switches **62** or **63** is turned OFF or ON at the timing when a TS packet #S2 is received as shown in FIG **6**F as described hereinabove, and the TS packet #S2 is supplied to the MUX **53** and subsequently supplied to the CPU **1** as described hereinafter.

On the other hand, it is assumed that the hard disk drive **15** reads out the recorded TS packets, and the reproduced transport stream that is sequential TS packets, for example, as shown in FIG. **6**G is thereby supplied from the transmitter **26** to the output PID parser **52**.

In the reproduced transport stream shown in FIG. 6G, it is assumed that the AV data loaded on a TS packet #AV3 is the AV data that is required to be reproduced, and the control data S1' loaded on a TS packet #S1' is the information necessary to reproduce the AV data AV3 loaded on the TS packet #AV3 (for example, PMT that describes the PID of a TS packet #AV3 or the like). Furthermore, it is assumed that the control data S4 loaded on a TS packet #S4 is unnecessary to reproduce the AV data AV3.

In this case, in the PID detecting unit **71** of the output PID parser **52** (FIG. 5A and FIG. 5B), the switch **72** is turned OFF at the timing when a TS packet #S4 is received as described hereinabove, and the TS packet #S4 is thereby discarded. Furthermore, in the PID detecting unit **71**, the switch **72** is turned ON at the timing when a TS packet #S1' and TS packet #AV3 are received, and the TS packets #S1' and AV3 are thereby supplied from the output PID parser **52** to the MUX **53** as shown in FIG. **6**H.

As described hereinabove, the TS packet S1 is supplied from the input PID parser **51** to the MUX **53** (FIG. **6**E), at that time if the PID of the TS packet #S1 is identical with the PID of the TS packet #S1' supplied from the output PID parser **52** to the MUX **53**, then the PID converting unit **73** of the output PID parser **52** (FIG. **5**A and FIG. **5**B) converts the PID of the TS packet #S1' as described hereinabove and thereafter supplies it to the MUX **53**. The shading in FIG. 6H and FIG. **6**I on the TS packets #S1' means that the PID of the TS packets #S1' shown in FIG. 6G has been changed.

The MUX **52** supplies the TS packet supplied from the output PID parser **52** to the switch **31** by way of the operator **55**.

Furthermore, the MUX **53** receives the TS packet from the output PID parser **52**, and receives the TA packets #S1 and #S2 from the input PID parser **51** as shown in FIG. 6E and FIG. 6F. Out of these TS packets, the timing when the TS packet #S1 is supplied from the input PID parser **51** overlaps with the timing when the output PID parser **52** sends out the TS packet #S1 as shown in FIG. 6H. Therefore, the TS packet #S1 sent out from the input PID parser **51** will collide with the TS packet #S1' sent out from the output PID parser **52** at the gate circuit **55** in the MUX **53** if the TS packet #S1 sent out from the input PID parser **51** and the TS packet #S1' sent out from the output PID parser **52** are supplied to the gate circuit **55** as they are.

To avoid such problem, if the timing when the input PID parser **51** sends out the TS packet to the gate circuit **55** overlaps with the timing when the output PID parser **52** sends out the TS packet to the gate circuit **55**, the addition control unit **54** of the MUX **53** shifts the output timing of the TS packet that is to be sent out by itself to there by prevent the collision between the TS packet sent out by itself and the TS packet sent out from the output PID parser **52** at the gate circuit **55**.

In detail, in this case, the addition control unit **54** temporarily stores the TS packet #S1 supplied from the input PID parser **51**, and sends out the stored TS packet S1 to the gate circuit **55** in a free time space when the TS packet is not sent out from the output PID parser **52** after the TS packet sent out from the output PID parser **52** passes through the gate circuit **55** as shown in FIG. **6**I. Thereby, the timing of the TS packet #S1 is shifted so that the TS packet #S1 does not collide with the TS packet sent out from the output PID parser **52**, and the TS packet #S1 is allowed to pass through the gate circuit **55**. As shown in FIG. 6F, because the timing when the TS packet #S2 supplied from the input PID parser **51** is supplied to the MUX **53** does not overlap with the timing when the TS packet supplied from the output PID parser **52** is supplied to the MUX **53**, the TS packet is sent out to the gate circuit **55** and the switch **31** without shifting of the timing.

The addition control unit **54** recognizes the free time space when the TS packet is not supplied from the output PID parser **52** to the gate circuit **55**. In detail, the addition control unit **54** communicates with the output PID parser **52** to thereby obtain the time stamp that is added to the TS packet to be sent out from the output PID parser **52**, and calculates the difference between the time stamp of the newest TS packet sent out from the output PID parser **52** and the time stamp of the TS packet that is to be sent out next to thereby recognize the free time space.

As described hereinabove, the MUX **53** supplies the transport stream that is sequential TS packets as shown in FIG. **6**I to the switch **31**.

In the case that the received transport stream is recorded and the transport stream recorded in the hard disk drive **15** is reproduced simultaneously, the switch **31** supplies the transport stream that is sequential TS packets supplied from the MUX **53** to the MVLink-IC **16** as the output transport stream, as the result the transport stream (FIG. **6**I) is isochronously transferred on the IEEE 1394 serial bus by way of the PHY-IC **17**, or sent out to the monitor by way of the DEMUX **18** and decoder **19**.

Therefore, because the control data S1' necessary to reproduce the AV data AV3 is supplied to the CPU **1** by way of the DEMUX **18**, the AV data AV3 is reproduced normally.

Furthermore, the control data S2 such as decoding key or the like used for descrambling is also supplied to the CPU 1 by way of the DEMUX **18**, as the result the descrambler **13** can descramble the transport stream supplied from the tuner **12**.

Furthermore, the control data S1 such as PMT or the like is supplied to the CPU 1 by way of the DEMUX **18** and the CPU 1 can thereby obtain the information or the like for knowing the status of the digital satellite broadcast in real time, and as the result occurrence of various problems is prevented.

As described hereinabove, in the digital satellite broadcast receiving apparatus, the received transport stream is recorded and the transport stream recorded in the hard disk drive **15** is reproduced simultaneously. As the result, for example, it is possible to perform the delayed playback, that is, while the received transport stream is being recorded in the hard disk drive **15**, the recorded transport stream is reproduced immediately. A user does not view the received transport stream as it is but can view the transport stream that is generated by recording temporarily and thereafter reproducing the received transport stream, in other words the user can view the time axis shifted received transport stream.

In the digital satellite broadcast apparatus shown in FIG. 1, a DEMUX having the same function as the DEMUX **18** is provided between the descrambler **13** and the PID parser **21**, and the DEMUX distributes the TS packet required to constitute the received transport stream to the DEMUX **18** and the PID parser **21**. Thereby, it is possible to perform simultaneous recording and reproduction of the transport stream as in the case of the digital satellite broadcast receiving apparatus shown in FIG. **2**. However, because the DEMUX **18** has the built-in CPU and memory or the like as described hereinabove, it is very expensive. Furthermore, because the DEMUX **18** is a component that is served for the complex processing such as analysis of the data loaded on the TS packet or the like, the additional DEMUX having the same function as that of the DEMUX **18** leads to a high cost and complex apparatus as a whole. On the other hand, the digital satellite broadcast receiving apparatus shown in FIG. **2** is inexpensive in the cost and simple in the structure in comparison with the apparatus having the additional DEMUX.

Next, the processing in the MUX **53** shown in FIG. **3** performed when the transport stream is recorded and reproduced simultaneously will be described hereinafter with reference to a flow chart shown in FIG. **7**.

In the MUX **53**, at first in step S1, whether the TS packet supplied from the output PID parser **52** (referred to as reproduced TS packet hereinafter properly) is received or the TS packet supplied from the input PID parser **51** (referred to as control TS packet hereinafter properly) is received is determined.

If whether the reproduced TS packet supplied from the input PID parser **52** is received or the control TS packet supplied from the input PID parser **51** is received is determined in step S1, then the sequence proceeds to step S2, and whether both reproduced TS packet and control TS packet are received or not in the MUX **53** is determined.

If it is determined that both the reproduced TS packet and the control TS packet are received in step S2, then the sequence proceeds to step S3, the addition control unit **54** stores the control TS packet supplied from the input PID parser **51** in the built-in buffer (not shown in the drawing), and the sequence proceeds to step S4. The gate circuit **55** supplies the reproduced TS packet supplied from the output PID parser **52** to the switch **31** in step S4, and the sequence returns to step S1.

On the other hand, if it is determined that both the reproduced TS packet and the control TS packet are not received in step S2, in other words, if it is determined that any one of the reproduced TS packet and the control TS packet is received, the sequence proceeds to step S5, and whether the received packet is either the reproduced TS packet supplied from the output PID parser **52** or the control TS packet supplied from the input PID parser **51** is determined in the MUX **53**. If it is determined that the received packet is the reproduced TS packet supplied from the output PID parser **52** in step S5, then the sequence proceeds to step S4, and the gate circuit **55** supplies the reproduced TS packet supplied from the output PID parser **52** to the switch **31** as described hereinabove, and the sequence returns to step S1.

On the other hand, if it is determined that the received packet is the control TS packet supplied from the input PID parser **51** in step S5, then the sequence proceeds to step S6, and whether the control TS packet is stored in the built-in buffer of the addition control unit **54** or not is determined. If it is determined that the control TS packet is stored in the control TS packet in the built-in buffer of the addition control unit **54** in step S6, then the sequence proceeds to step S7, and the addition control unit **54** stores the received control TS packet in the built-in buffer and reads out the oldest control TS packet from among control TS packets stored already in the buffer (the control TS packet that has been stored first), and supplies it to the gate circuit **55**, and the sequence returns to step S1. Thereby, the control TS packet stored in the buffer of the addition control unit **54** is supplied from the gate circuit **55** to the switch **31**.

On the other hand, if it is determined that the control TS packet is not stored in the buffer of the addition control unit **54** in step S6, the sequence proceeds to step S8, and the addition control unit **54** supplies the received control TS packet to the gate circuit **55**, and the sequence returns to step S1. Thereby, the control TS packet supplied from the input PID parser **51** is supplied from the gate circuit **55** to the switch **31**.

On the other hand, if it is determined that neither the reproduced TS packet supplied from the output PID parser **52** nor the control TS packet supplied from the input PID parser **51** is received in step S1, in other words if it is determined that there is a free time space as described hereinabove, then the sequence proceeds to step S9, and whether the control TS packet is stored in the built-in buffer of the addition control unit **54** or not is determined. If it is determined that the control TS packet is not stored in the built-in buffer of the addition control unit **54**, then the sequence returns to step S1, and the same processing is repeated subsequently.

If it is determined that the control TS packet is stored in the built-in buffer of the addition control unit **54** in step S9, then the sequence proceeds to step S10, and the addition control unit **54** reads out the oldest control TS packet from among control TS packets stored in the built-in buffer and supplies it to the gate circuit **55**, and the sequence returns to step S1. Thereby, the control TS packet stored in the buffer of the addition control unit **54** is supplied from the gate circuit **55** to the switch **31**.

The above-mentioned series of processing can be implemented not only by means of the hardware but also by means of the software. In the case that the series of processing is implemented by means of the software, a program that constitutes the software is installed in a computer or a

general-purpose computer that is incorporated in a digital satellite broadcast receiving apparatus served as the exclusive hardware.

A recording medium in which the program to be installed in a computer for enabling the computer to execute the above-mentioned series of processing is recorded will be described with reference to FIG. **8**A to FIG. **8**C.

The program may be stored previously in a hard disk **102** or semiconductor memory **103** provided as the built-in recording medium in the computer **101** as shown in FIG. **8**A.

Otherwise, the program may be stored temporarily or permanently in a recording medium such as a floppy disc **111**, a CD-ROM (Compact Disc Read Only Memory) **112**, an MO (Magneto-optical) disc **113**, a DVD (Digital Versatile Disc) **114**, a magnetic disc **115**, or a semiconductor memory **116** as shown in FIG. **8**B. Such recording medium is provided as so-called package software.

The program may be transferred wirelessly to the computer **101** from a download site **121** by way of a digital satellite broadcasting artificial satellite **122** as shown in FIG. **8**C in addition to a method in which the program is installed from a recording medium as described hereinabove, and further otherwise the program may be transferred to the computer through a wire by way of LAN (Local Area Network) or a network such as the Internet and installed in the built-in hard disk **102** of the computer **101**.

In the present specification, the processing step for describing the program for performing various processing by means of the computer is not necessarily implemented in the order of time series described in the flow chart, and includes parallel processing or processing to be implemented separately (for example, parallel processing or processing by means of object).

The program may be processed by means of a single computer or may be processed separately by means of a plurality of computers. Furthermore, the program may be transferred to a computer located remotely and implemented therein.

Next, FIG. **9** shows an exemplary structure of the computer **101** shown in FIG. **8**A to FIG. **8**C.

The computer **101** has a built-in CPU (Central Processing Unit) **142** as shown in FIG. **9**. The CPU **142** is connected to the input/output interface **145** by way of the bus **141**. When a user enters a command by operating an input unit **147** having a key board and mouse or the like as the component by way of the input/output interface **145**, the CPU **142** loads the program stored in the ROM (Read Only Memory) **143** corresponding to the semiconductor memory **103** shown in FIG. **8**A. Otherwise, the CPU **142** loads the program stored in the hard disk **102**, the program that has been transferred from the satellite **122** or network **131** and received by means of the communication unit **148** and installed in the hard disk **102**, or the program that has been read out from the floppy disc **111** mounted on the drive **149**, the CD-ROM **112**, the MO disc **113**, the DVD **114**, or the magnetic disc **115** and installed in the hard disk **102** on the RAM (Random Access Memory), and the CPU **142** executes the program. Then, the CPU **142** sends out the processing result to, for example, the display unit comprising a LCD (Liquid Crystal Display) or the like as required by way of the input/output interface **145**.

In the present embodiment, the present invention is described in respect to the digital satellite broadcast receiving apparatus for receiving the digital satellite broadcast wave to which the present invention is applied, however, the present invention may be applied to any apparatus that receives the digital data.

In the present embodiment, the digital satellite broadcast receiving apparatus having the built-in hard disk drive **15** is described, however, the hard disk drive **15** may be of a detachable type.

In the present embodiment, in the case that the PID of the TS packet supplied from the input PID parser **51** is identical with the PID of the TS packet supplied from the output PID parser **52**, the output PID parser **52** converts the PID of the TS packet that is to be sent out from the output PID parser **52** itself, however, the input PID parser **51** may converts the PID of the TS packet that is to be sent out from the input PID parser **51** itself. In other words, in the case that the PID of the TS packet that constitutes the transport stream transferred as the digital satellite broadcast program is known previously, the input PID parser **51** can convert the PID of the TS packet that constitutes the received transport stream supplied thereto so that the coincidence of PID does not occur as described hereinabove.

The transport stream described in the present specification may include not only the stream having 188 byte TS packets but also, for example, the stream or the like having 130 byte packets, which is used for DSS (Direct Satellite System) by DirecTV company in the US and decoded in the same principle as used for decoding the TS packet.

According to the data processing apparatus and data processing method, and the recording medium of the present invention, at least the first packet to be only recorded, the second packet to be recorded and to be used for controlling, and the third packet to be used only for controlling are extracted from among the packets that constitute the received stream. The first and second packets are supplied to a recording apparatus served for recording the data, and the second packet, the third packet, and the packet reproduced from the recording apparatus are multiplexed, and the multiplexed packet is sent out. As the result, it is possible to record the packet and reproduce the recorded packet simultaneously.

What is claimed is:

1. A data processing apparatus for receiving and processing a stream having packets of a predetermined format comprising:

packet extracting means at least for extracting a first packet only to be recorded, a second packet to be recorded and to be used for controlling, and a third packet to be used only for controlling from among component packets of said received stream;

packet output means for supplying said first and second packets to a recording unit for recording the data;

multiplexing means for multiplexing said second and third packets and a packet reproduced from said recording unit and for sending out the multiplexed packet; and

converting means for converting the PID of any one of said second or third packet and the packet reproduced from said recording unit when the PID (Packet Identification) of said second or third packet is identical with that of the packet reproduced from said recording unit.

2. A data processing apparatus as claimed in claim **1**, wherein said stream comprising packets of the predetermined format is a transport stream.

3. A data processing apparatus as claimed in claim **1**, wherein when said multiplexing means receives said second or third packet and said packet reproduced from said recording unit simultaneously, said multiplexing means:

temporarily stores said second or third packet and sends out said packet reproduced from said recording unit; and

sends out said stored second or third packet when said packet reproduced from said recording unit is not received.

4. A data processing apparatus as claimed in claim 1, wherein said recording unit is further incorporated in said data processing apparatus.

5. A data processing method for receiving and processing a stream having packets of a predetermined format, comprising the steps of:

extracting at least a first packet only to be recorded, a second packet to be recorded and to be used for controlling, and a third packet to be used only for controlling from among component packets of said received stream;

supplying said first and second packets to a recording unit for recording the data;

multiplexing said second and third packets and a packet reproduced from said recording unit and of sending out the multiplexed packet; and

converting the PID of any one of the packets when PID (Packet Identification) of said second or third packet is identical with PID of the packet reproduced from said recording unit.

6. A data processing method as claimed in claim 5, wherein said multiplexing step, when said multiplexing step receives said second or third packet and the packet reproduced from said recording unit simultaneously, temporarily stores said second or third packet and sends out the packet reproduced from said recording unit, and sends out the stored said second or third packet while the packet reproduced from said recording unit is not being received.

7. A recording medium in which a program for controlling a computer to receive and process a stream having packets of a predetermined format contains a recorded program comprising:

packet extracting means at least for extracting a first packet only to be recorded, a second packet to be recorded and to be used for controlling, and a third packet to be used only for controlling from among component packets of said received stream;

packet output means for supplying said first and second packets to a recording unit for recording the data;

multiplexing means for multiplexing said second and third packets and a packet reproduced from said recording unit and of sending out the multiplexed packet; and

converting means for converting the PID of any one of said second or third packet and the packet reproduced from said recording unit when the PID (Packet Identification) of said second or third packet is identical with that of the packet reproduced from said recording unit.

8. A digital broadcast receiving apparatus having a built-in storage device for recording the data comprising:

first discrimination means for discriminating whether the received transport stream is a transport stream for recording and controlling, a transport stream only for recording, or a transport stream only for controlling;

second discrimination means for discriminating whether the transport stream reproduced from said storage device is to be sent out or to be discarded; and

comparison means for comparing the identification ID in said transport stream for controlling the identification ID in said reproduced and sent out predetermined transport stream;

wherein the transport stream recorded in said storage device is reproduced while the received transport stream is being recorded.

9. A digital broadcast receiving apparatus as claimed in claim 8, wherein said storage device is a hard disk.

10. A digital broadcast receiving apparatus as claimed in claim 8, wherein said first and second discrimination means discriminate based on the identification ID in the transport stream.

11. A digital broadcast receiving apparatus as claimed in claim 8, wherein said first discrimination means further discriminates whether said transport stream is a transport stream to be discarded or not.

12. A digital broadcast receiving apparatus as claimed in claim 8, comprising conversion means for converting the identification ID in said reproduced and sent out predetermined transport stream when said comparison means determines both identification IDs to be identical with each other.

13. A digital broadcast receiving apparatus as claimed in claim 8, further comprising a multiplexing means for multiplexing said transport stream for recording and controlling, said transport stream only for controlling, and said transport stream reproduced from said storage device.

14. A digital broadcast receiving apparatus as claimed in claim 13, wherein said multiplexing means adjusts the output timing so that said multiplexed transport streams does not collide with one another.

15. A recording/reproducing method used in a digital broadcast receiving apparatus having a built-in storage device for recording the data, comprising the steps of:

discriminating whether the received transport stream is a transport stream for recording and controlling, a transport stream only for recording, or a transport stream only for controlling;

discriminating whether the transport stream reproduced from said storage device is to be sent out or to be discarded;

comparing the identification ID in said transport stream for controlling with the identification ID in said reproduced and sent out predetermined transport stream; and

converting the identification ID in said reproduced and sent-out predetermined transport stream when said comparison means determines both identification IDs to be identical with each other;

wherein the transport stream recorded in said storage device is reproduced while the received transport stream is being recorded.

16. A recording/reproducing method used in a digital broadcast receiving apparatus as claimed in claim 15, further comprising a multiplexing step of multiplexing said transport stream for recording and controlling, said transport stream only for controlling, and said transport stream reproduced from said storage device.

* * * * *

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	William B. Boyle
Appl. No.	:	09/747,002
Filed	:	December 22, 2000
For	:	METHOD AND APPARATUS FOR STORING A STREAM OF VIDEO DATA ON A STORAGE MEDIUM
Examiner	:	Jamie J. Vent
Group Art Unit	:	2616

DECLARATION OF WILLIAM B. BOYLE PURSUANT TO 37 C.F.R.§ 1.132

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, William B. Boyle, declare as follows:

1. I am the sole inventor of the claimed subject matter of the above-captioned patent application.

2. I have reviewed the above-captioned patent application, including the specification, the originally-filed claims, and the currently-pending claims. I have also reviewed the September 13, 2005 Final Office Action and the November 17, 2005 Advisory Action in the above-captioned patent application, including the rejection of Claims 17-29 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,134,384 issued to Okamoto et al. ("Okamoto") in view of U.S. Patent No. 6,792,000 issued to Morinaga et al. ("Morinaga"). I have also reviewed the Okamoto and Morinaga references.

3. Okamoto discloses a system and method for recording on and reproducing from a magnetic tape a digital signal using a plurality of rotating heads. Because magnetic tape is a sequentially-accessed storage medium, it cannot be randomly accessed, as can hard disk drives. Furthermore, data is formatted on magnetic tape in sequential parallel linear tracks, each track

comprising various blocks with subareas containing various datafields. Okamoto discloses adding error correction codes to digital signals being recorded onto the magnetic tape using a first rotating head and reproducing the recorded signal and the added error correction codes using a second rotating head concurrently with the recording of the signal onto the magnetic tape. The system disclosed by Okamoto uses the reproduced error correction codes to detect errors in the reproduced signal. In this way, Okamoto discloses a system and method for confirming the accuracy of digital signals recorded onto a sequentially-accessed medium such as magnetic tape.

4. Morinaga discloses a system and method for recording transport streams onto a hard disk drive, which is a non-sequentially-accessed storage medium. Such hard disk drives typically have one or more platters, each platter being used only with a single read/write head. Data is formatted on the platters in concentric circular tracks, each track comprising a plurality of sectors. The hard disk drive is addressable on boundaries between the sectors.

5. Because the hard disk drive disclosed by Morinaga is a non-sequentially-accessed storage medium, a single head can be directed to a particular portion of the corresponding platter to confirm the accuracy of a particular recorded signal. There is no need for a plurality of heads to concurrently record digital signals and confirm the accuracy of the recorded digital signals on the hard disk drive, as there is for the sequentially-accessed storage medium (magnetic tape) disclosed by Okamoto.

6. Persons skilled in the art would not be motivated to combine the hard disk drive disclosed by Morinaga with the system and method disclosed by Okamoto since hard disk drives as disclosed by Morinaga do not require the simultaneous playback for confirming the accuracy of signals recorded on magnetic tape as disclosed by Okamoto.

7. Because of the differences between the sequentially-accessed medium of magnetic tape and the non-sequentially-accessed medium of a hard disk drive, including differences in the data formats of these two types of media, the hard disk drive disclosed by Morinaga cannot be easily substituted for the magnetic tape disclosed by Okamoto. Such a substitution would require changing the data formats disclosed by Okamoto from those of sequentially-accessed media to those of non-sequentially-accessed media. Such a substitution would also require changing the mechanisms which record and reproduce the signals and the added error correction codes. Thus, combining the disclosure of Morinaga with the disclosure of Okamoto would require a

substantial reconstruction and redesign of the elements shown in the Okamoto reference as well as a change in the basic principle under which the system and method of Okamoto was designed to operate.

8. As disclosed by the present application at page 6, lines 6-10, in certain embodiments, the claimed invention of the present application provides modified transport packets which "align[] more often with the first byte of a sector so that the system 1 can more efficiently access the video data" stored on the hard disk drive and to enable "trick play" functions (such as fast forward, reverse, rewind, skip) without loss of synchronization. This more frequent alignment and smaller cluster size "provides for more efficient access to the stored video data because the synchronization performance is improved and repeated re-locking of a decoder ... is avoided." (*see*, present application at page 7, lines 20-23.) In contrast, neither Okamoto nor Morinaga discloses or suggests such an advantage, and persons skilled in the art would not expect such an advantage from the combination of Okamoto in view of Morinaga.

9. I hereby declare that all statements made herein of my own knowledge are true, and that all statements made upon information and belief are believed to be true; and further, that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001, Title 18 of the United States Code, and that willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

Dated: 12/19/05 By: William B. Boyle
William B. Boyle

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